TAMAGAWA SEIKI CO.,LTD.

Smartcoder®

AU6802N1

USERS MANUAL

MNL000392W00

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Safety Matters

Before use AU6802N1, please carefully read the specification and this manual for proper use. Incorrect usage do not operate normally, may damage the equipment that is connected to this product or this product.
Retained for this manual, please re-read when you do not know.

■Notes

Smartcoder (AU6802N1) is an integrated circuit (i.e electronic device) with a high grade quality level suitable for use in automobiles, trains, etc. and is designed for units involving direct control and safety of transportation equipment. But the calculated failure rate is not zero. Also there are some possibility to do unplanned work cause of noise, static electricity, wiring error, etc. Therefore, the customer is to assume this responsibility, considering the possibility of failure, and to design multiple back-up solutions within the equipment or system to avoid a serious system failure.

These application samples which listed in this manual are reference examples. If you use these examples, please make sure that you understand your system, equipments, and those functions and safety.

The information contained in this manual might be changed as necessary. For the latest content, please contact your local sales representative.

■Product Warranty

(1)Warranty Period

The warranty period for Smartcoder (AU6802N1) is one year after shipping. Failed products within this warranty period will be replaced with new one.

(2)Coverage

Even if within the warranty period, we will not take responsibility for the products which show quality degradation caused by deviant usage against this document or specification like below.

- In case of usage of unguaranteed condition/environment/handling nonlisted in this manual or specification.
- In case of Remodeling/Repair which is not done by Tamagawa-seiki.
- In case of misusing this product.
- In case of unforeseen matters which can not expect at technology level of shipping age.

1. Introduction

1.1 Product Overview

Smartcoder(AU6802N1) is an R/D (Resolver to Digital) conversion IC used with a brushless Resolver such as Singlsyn, Smartsyn, etc. It converts the electrical information (analog signal) corresponding to a mechanical rotational angle of the Resolver to the corresponding digital data and transmits it.

It was developed as simple usage, low cost, and having high quality enough to be used on vehicles, while maintaining high reliability that the Resolver (Synchro) system has had conventionally. It provides you wide range applications for angle detection.

1.2 Product Features

■Wide operating temperature range for automotive quality:−40℃～+125℃

■Real time output:High tracking rate:240,000min^{-1}(10Bit resolution)

■Single power supply of DC+5V

■Small size /light weight:10×10mm(Pin interval 0.65mm、52pin TQFP、Mass 0.3g)

■Built-in test to detect following faults:
abnormal sensor signal、abnormal R/D conversion

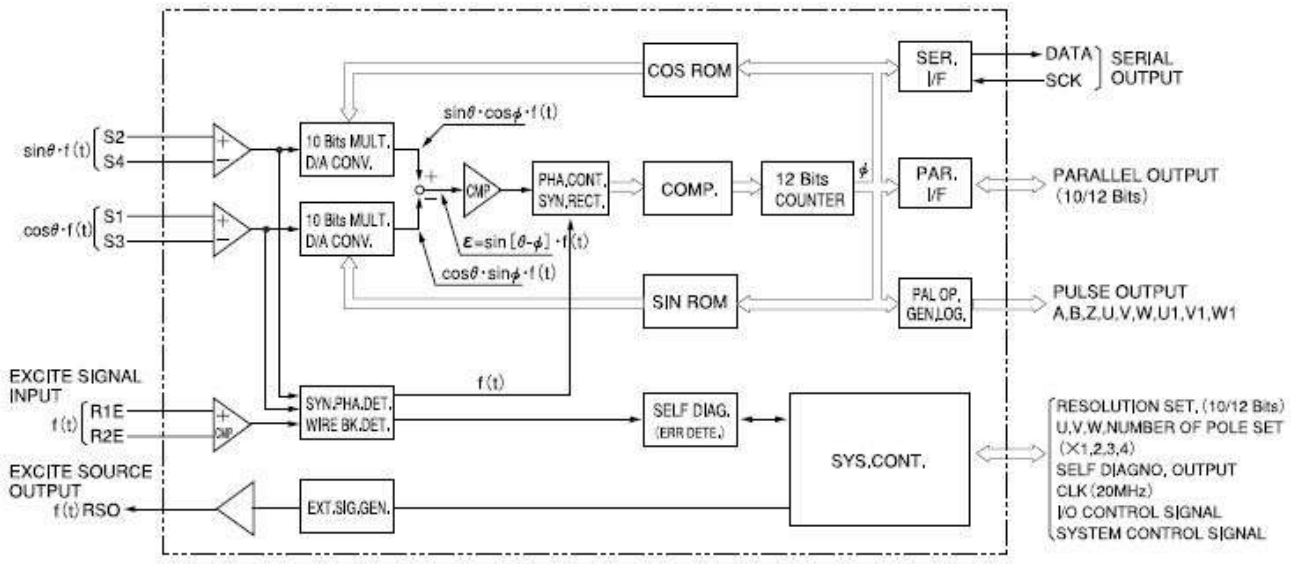
■Selectable output mode : Pulse/Parallel/Bus + Serial output

■Selectable resolution mode:10Bit/12Bit

■Selectable setting a number of poles for UVW: ×1,2,3,4

■ Selectable clock input(20MHz):
External CLK input/Crystal resonator/Ceramic resonator

1.3 Block Diagram



1.4 Spec Overview

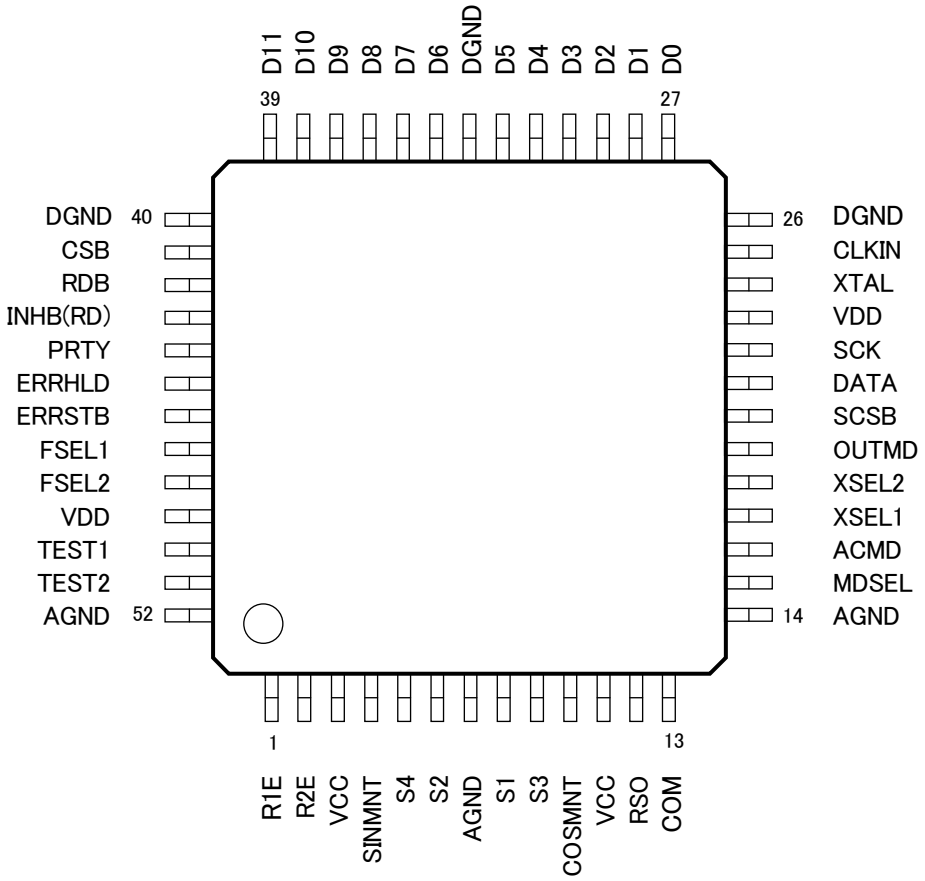
Output form		Binary code parallel 10／12bit bus compatible、positive logic	
Resolution		1,024 (2^{10})	4,096 (2^{12})
Conversion accuracy (Static)		±2 LSB	±4 LSB
Settling time (For step input of 180° in electric angle)	ACMD="H"	1 ms Typ.	2.5 ms Typ.
	ACMD="L"	15 ms Typ.	60 ms Typ.
Max. tracking rate		240,000 min^{-1}	60,000 min^{-1}
Max. angular acceleration		256,000 rad / s^2	64,000 rad / s^2
Response (As output response delay in electric angle)		±0.2° Max./10,000 min^{-1}	±0.4° Max./10,000 min^{-1}
Encoder emulation output (A,B)		256 C/T	1,024 C/T
Fault detection function		・abnormal sensor signal(EX: breaking/down of exciting sourse lines, Breaking of Resolver signal lines) ・abnormal R/D conversion	
Power source		DC 5V±5% 45mA Max. (30mA Typ.)	
Operating temperature		−40 ～ +125℃	
Storage temperature		−65 ～ +150℃	
Humidity		90% RH Max.	
Mass		1g max	

1.5 Related documents

（1） 80110141114E　　Smartcoder(AU6802N1) specification

2. Pin List (Name and Functions)

2.1 Pin Assignment



2.2 Pin Description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Class</th><th>Description</th><th>Remarks</th></tr>
<tr><td>1</td><td>R1E</td><td>A／I</td><td>External exciting signal input(R1).</td><td rowspan="2">(Ref:4.2.3)</td></tr>
<tr><td>2</td><td>R2E</td><td>A／I</td><td>External exciting signal input(R2).</td></tr>
<tr><td>3</td><td>VCC</td><td>——</td><td>Analog power pin. Connect to +5V.</td><td>(Ref:4.5)</td></tr>
<tr><td>4</td><td>SINMNT</td><td>A／O</td><td>Resolver signal (SIN) monitor output. Input gain should be adjusted to be approximately 2~3 Vp-p for this pin.</td><td rowspan="3">(Ref:4.2.2)</td></tr>
<tr><td>5</td><td>S4</td><td>A／I</td><td>Resolver signal(S4) input pin.</td></tr>
<tr><td>6</td><td>S2</td><td>A／I</td><td>Resolver signal(S2) input pin.</td></tr>
<tr><td>7</td><td>AGND</td><td>——</td><td>Analog ground pin. Connect to 0V.</td><td>(Ref:4.5)</td></tr>
<tr><td>8</td><td>S1</td><td>A／I</td><td>Resolver signal(S1) input pin.</td><td rowspan="3">(Ref:4.2.2)</td></tr>
<tr><td>9</td><td>S3</td><td>A／I</td><td>Resolver signal(S3) input pin.</td></tr>
<tr><td>10</td><td>COSMNT</td><td>A／O</td><td>Resolver signal(COS) monitor output. Input gain should be adjusted to be approximately 2~3 Vp-p for this pin.</td></tr>
<tr><td>11</td><td>VCC</td><td>——</td><td>Analog power pin. Connect to +5V.</td><td>(Ref:4.5)</td></tr>
<tr><td>12</td><td>RSO</td><td>A／O</td><td>Exciting signal output pin. Output signal should be 2Vp-p± 10% which center voltage is “COM” pin level. This signal will be used for input of exciting voltage booster amplifier</td><td rowspan="2">(Ref:4.2.1)</td></tr>
<tr><td>13</td><td>COM</td><td>A／O</td><td>COM output pin. Output is “0.5×VCC±5%” voltage.
It must be 470pF decoupling capacitor between COM-pin and RSO-pin.</td></tr>
<tr><td>14</td><td>AGND</td><td>——</td><td>Analog ground pin. Connect to 0V.</td><td>(Ref:4.5)</td></tr>
<tr><td>15</td><td>MDSEL</td><td>D／I</td><td>Resolution selection pin.<table><tr><th>Resolution</th><th>10 Bit</th><th>12 Bit</th></tr><tr><td>MDSEL</td><td>H</td><td>L</td></tr></table></td><td>(Ref:4.3.1)</td></tr>
<tr><td>16</td><td>ACMD</td><td>D／I</td><td>Internal control mode selection pin.<table><tr><th>Acc. Mode</th><th>ON</th><th>OFF</th></tr><tr><td>ACMD</td><td>H</td><td>L</td></tr></table></td><td>(Ref:4.3.1)
(Ref:10.2)</td></tr>
<tr><td>17</td><td>XSEL1</td><td>D／I</td><td rowspan="2">Number of poles (UVW) selection pin.
These pins control to U1,V1,W1signals.<table><tr><th>No of pole</th><th>X1</th><th>X2</th><th>X3</th><th>X4</th></tr><tr><td>XSEL1</td><td>H</td><td>L</td><td>H</td><td>L</td></tr><tr><td>XSEL2</td><td>H</td><td>H</td><td>L</td><td>L</td></tr></table></td><td rowspan="2">(Ref:4.3.1)</td></tr>
<tr><td>18</td><td>XSEL2</td><td>D／I</td></tr>
<tr><td>19</td><td>OUTMD</td><td>D／I</td><td>Parallel output (D0~D11) mode selection pin.<table><tr><th>Output mode</th><th>Absolute-mode</th><th>Pulse-mode</th></tr><tr><td>OUTMD</td><td>H</td><td>L</td></tr></table></td><td>(Ref:4.3.1)
(Ref:4.3.2(1))
(Ref:4.3.2(2))
(Ref:4.3.2(4))</td></tr>
<tr><td>20</td><td>SCSB</td><td>D／I</td><td>Chip selection pin for serial output. It controls DATA pin mode and serial out data will be latched at SCSB falling edge<table><tr><th>DATA pin mode</th><th>Valid</th><th>High impedance</th></tr><tr><td>SCSB</td><td>L</td><td>H</td></tr></table></td><td rowspan="3">(Ref:4.3.2(3))
(Ref:4.3.2(4))</td></tr>
<tr><td>21</td><td>DATA</td><td>D/O(BUS)</td><td>Serial data output pin. The data which is absolute angle data at falling edge of SCSB is transmitted with SCK.</td></tr>
<tr><td>22</td><td>SCK</td><td>D／I</td><td>Serial clock input pin. It is used the serial output function. Frequency is 2MHz (max.).</td></tr>
<tr><td>23</td><td>VDD</td><td>——</td><td>Digital power pin. Connect to +5V.</td><td>(Ref:4.5)</td></tr>
<tr><td>24</td><td>XTAL</td><td>——</td><td>Oscillator connection pin.</td><td>(Ref:4.4)</td></tr>
<tr><td>25</td><td>CLKIN</td><td>D／I</td><td>External clock input pin. Frequency of the device to be connected is 20MHz.</td><td>(Ref:4.4)</td></tr>
<tr><td>26</td><td>DGND</td><td>——</td><td>Digital ground pin. Connect to 0V.</td><td>(Ref:4.5)</td></tr>
</table>

(Note) “Class” means as follow.

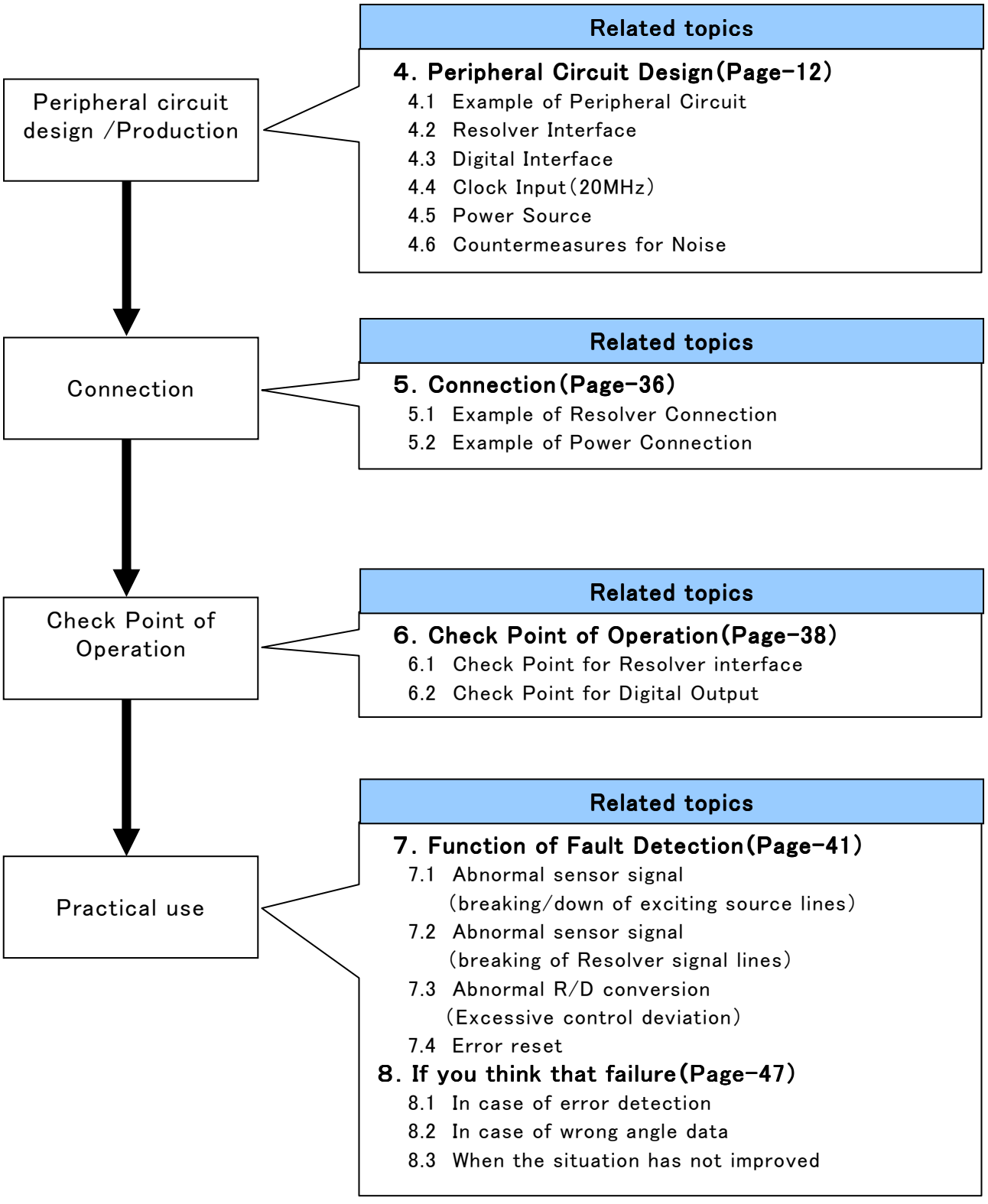
* A／I : Analog input
* A／O : Analog output
* D／I : Digital input
* D／O(BUS) : Digital output(3-state output)

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Class</th><th>Description</th><th>Remarks</th></tr>
<tr><td>27</td><td>D 0</td><td>D/O(BUS)</td><td>OUTMD = H: φ12 (12Bit LSB)
OUTMD = L: PRTY</td><td rowspan="6">(Ref:4.3.1)
(Ref:4.3.2(1))
(Ref:4.3.2(2))
(Ref:4.3.2(4))</td></tr>
<tr><td>28</td><td>D 1</td><td>D/O(BUS)</td><td>φ11 / ERRHLD</td></tr>
<tr><td>29</td><td>D 2</td><td>D/O(BUS)</td><td>φ10 (10Bit LSB) / ERR</td></tr>
<tr><td>30</td><td>D 3</td><td>D/O(BUS)</td><td>φ9 / W1</td></tr>
<tr><td>31</td><td>D 4</td><td>D/O(BUS)</td><td>φ8 / V1</td></tr>
<tr><td>32</td><td>D 5</td><td>D/O(BUS)</td><td>φ7 / U1</td></tr>
<tr><td>33</td><td>DGND</td><td>——</td><td>Digital ground pin. Connect to 0V.</td><td>(Ref:4.5)</td></tr>
<tr><td>34</td><td>D 6</td><td>D/O(BUS)</td><td>OUTMD = H: φ6
OUTMD = L: W</td><td rowspan="6">(Ref:4.3.1)
(Ref:4.3.2(1))
(Ref:4.3.2(2))
(Ref:4.3.2(4))</td></tr>
<tr><td>35</td><td>D 7</td><td>D/O(BUS)</td><td>φ5 / V</td></tr>
<tr><td>36</td><td>D 8</td><td>D/O(BUS)</td><td>φ4 / U</td></tr>
<tr><td>37</td><td>D 9</td><td>D/O(BUS)</td><td>φ3 / Z</td></tr>
<tr><td>38</td><td>D10</td><td>D/O(BUS)</td><td>φ2 / B</td></tr>
<tr><td>39</td><td>D11</td><td>D/O(BUS)</td><td>φ1 (MSB) / A</td></tr>
<tr><td>40</td><td>DGND</td><td>——</td><td>Digital ground pin. Connect to 0V.</td><td>(Ref:4.5)</td></tr>
<tr><td>41</td><td>CSB</td><td>D／I</td><td rowspan="2">Chip selection pin(CSB) and Read pin(RDB). D0~D11 and PRTY output state can be controlled.
D0~D11,PRTY out: CSB, RDB — Valid: L, L — High impedance: Other combination</td><td rowspan="3">(Ref:4.3.2(1))
(Ref:4.3.2(2))</td></tr>
<tr><td>42</td><td>RDB</td><td>D／I</td></tr>
<tr><td>43</td><td>INHB(RD)</td><td>D／I</td><td>Inhibit pin.
D0~D11 signal data state (Through/Hold) can switch.
D0~D11 signals: INHB(RD) — Through: H — Hold: L</td></tr>
<tr><td>44</td><td>PRTY</td><td>D/O(BUS)</td><td>This is even parity signal of the parallel output data. φ1~φ12(12Bit-mode) Or φ1~φ10(10Bit-mode), in case of the number of “H” level data is even, this pin output as “L”.</td><td></td></tr>
<tr><td>45</td><td>ERRHLD</td><td>D／O</td><td>Error state hold pin. Once this devise detect fault condition, this pin output will be changed to “H” and keep it.</td><td rowspan="2">(Ref: 8)</td></tr>
<tr><td>46</td><td>ERRSTB</td><td>D／I</td><td>Error reset pin. This signal reset the ERRHLD output state.
ERRHLD signal: ERRSTB — HOLD: H — Clear HOLD state: L</td></tr>
<tr><td>47</td><td>FSEL1</td><td>D／I</td><td rowspan="2">RSO output frequency selection pin.
RSO freq.: FSEL1, FSEL2 — 20kHz: H, H — 10kHz: L, H — –: Other combination</td><td rowspan="2">(Ref:4.3.1)</td></tr>
<tr><td>48</td><td>FSEL2</td><td>D／I</td></tr>
<tr><td>49</td><td>VDD</td><td>——</td><td>Digital power pin. Connect to +5V.</td><td>(Ref:4.5)</td></tr>
<tr><td>50</td><td>TEST1</td><td>D／I</td><td rowspan="2">These pins do not affect the operation directly. Connect to the digital power (VDD).</td><td rowspan="2"></td></tr>
<tr><td>51</td><td>TEST2</td><td>D／I</td></tr>
<tr><td>52</td><td>AGND</td><td>——</td><td>Analog ground pin. Connect to 0V.</td><td>(Ref:4.5)</td></tr>
</table>

(Note) “Class” means as follow.

* D／ I : Digital input
* D／O : Digital output
* D／O(BUS) : Digital output(3-state output)

3. Setup Flow


Peripheral circuit design /Production
Related topics
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4.2 Resolver Interface
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4.4 Clock Input(20MHz)
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5.2 Example of Power Connection
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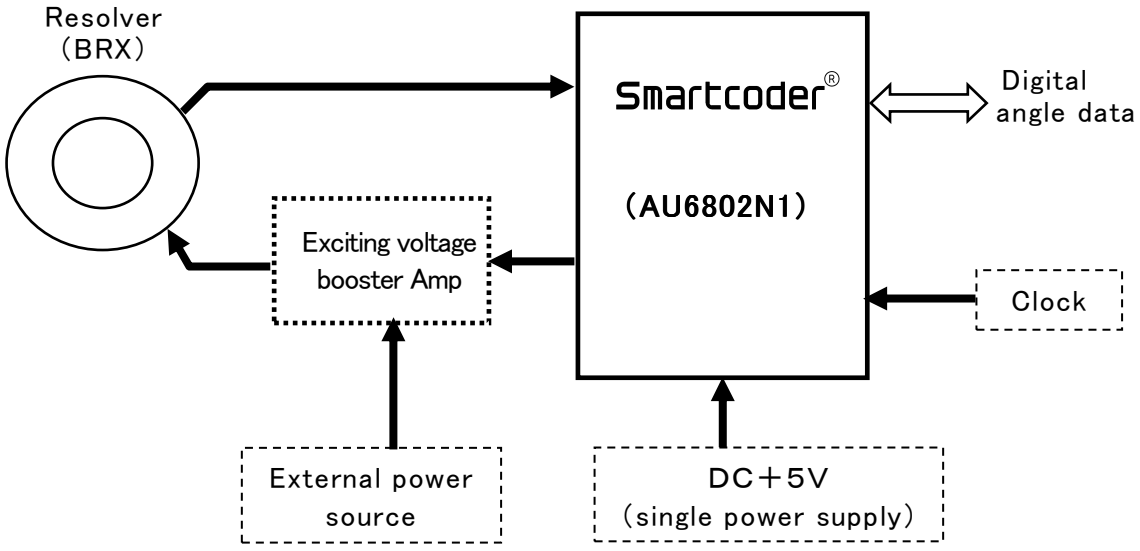
8.3 When the situation has not improved

4. Peripheral Circuit Design

AU6802N1 require some peripheral circuit to get digital angle data. In this chapter, we explain the design method and important point for required peripheral circuit design.

4.1 Example of Peripheral Circuit



4.2 Resolver Interface

※ Examples mentioned in this articles shows only the concept of basic functions. Please note that each application might have their each individual requirement. Therefore the circuit configuration and the decision of constants for practical resistors and the function of protection for input/output circuits, etc. should be designed for each application.

4.2.1 Excitation Amplifier Circuit

Resolver (BRX type) is the sensor which generates the amplitude signal responding to the rotational angle of output winding by applying excitation signal to excitation windings. Then exciting amplifier circuit to excite resolver need to get resolver output signals.

There are 2 type of excitation amplifier circuit, current control type and voltage control type. Show merit/demerit of each method in below. Please determine appropriate method for your system considering them.

Excitation Amp.	Merit	Demerit
Current control type	・Prevention of secondary failure(damage of output TR, etc.) by short circuit between exciting lines. ・Less temperature change of resolver signal due to constant current.	・Circuit is getting complex, and it might not operate as calculations. ・Exciting voltage might vary due to resolver input impedance variability.
Voltage control type	・Circuit is simple and it will operate as calculations. ・Exciting voltage can be constant.	・possibility to have secondary failure due to overcurrent by short circuit between exciting lines. ・There might have temperature change of resolver signal.

Separate power supply (V_{ext}) is required for the excitation amplifier circuit, in addition to the AU6802N1 (+5V) power supply.

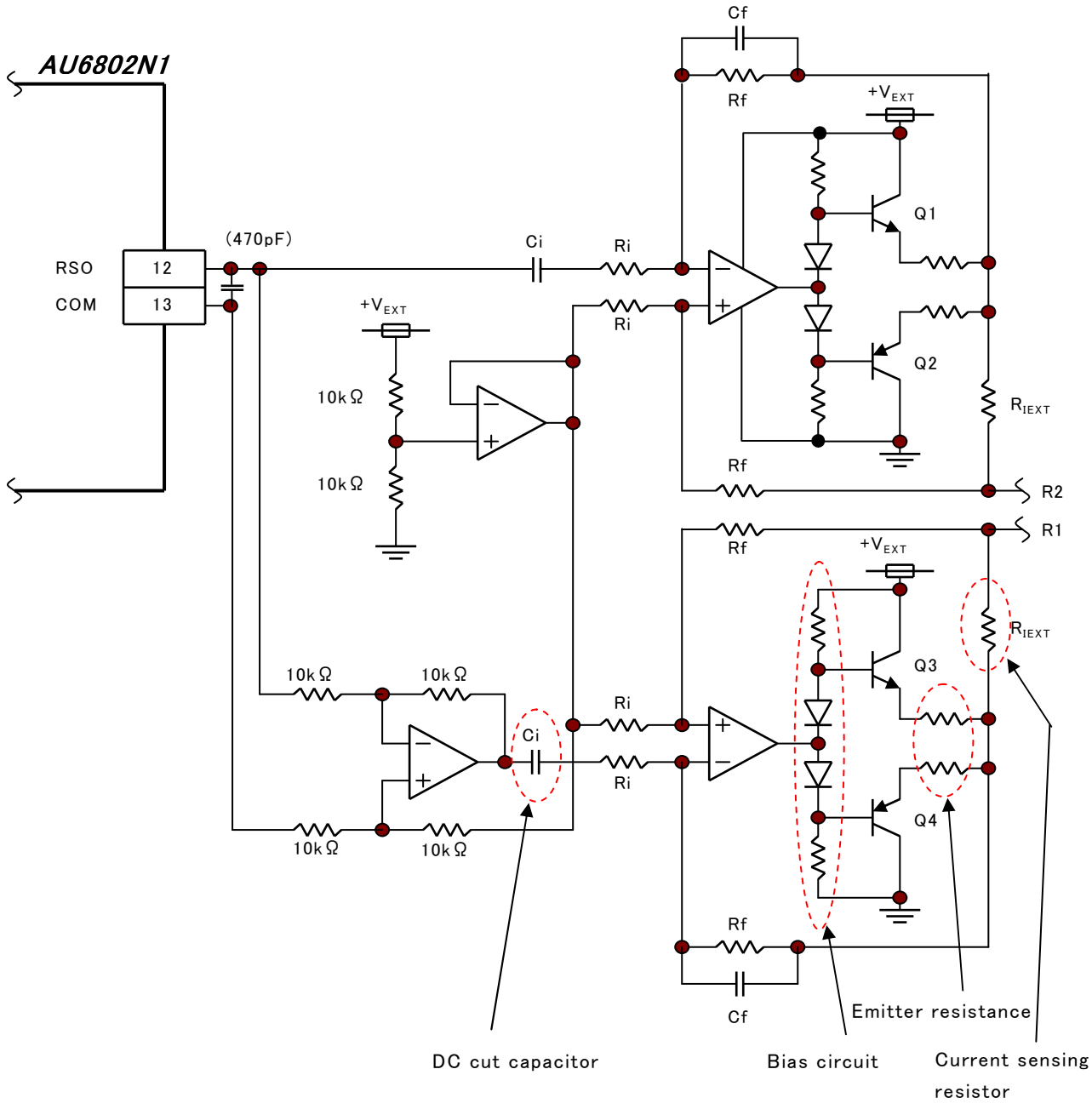
Higher resolver exciting voltage caused higher resolver output voltage, and it can expect to improve the S/N ratio or noise immunity. That mean it need appropriate DC power supply. For example, exciting voltage 7Vrms(=20V_{p-p} :7V×√2×2) require ＋24V for single power source or ±15V for dual power sources.

Resolver operation will be possible at the lower exciting voltage compared to the value described in the specification. So please decide exciting voltage value considering noise immunity and power equipment which can be prepared.

In this chapter, we will show you the example of excitation amplifier circuit (current control type) using RSO output.

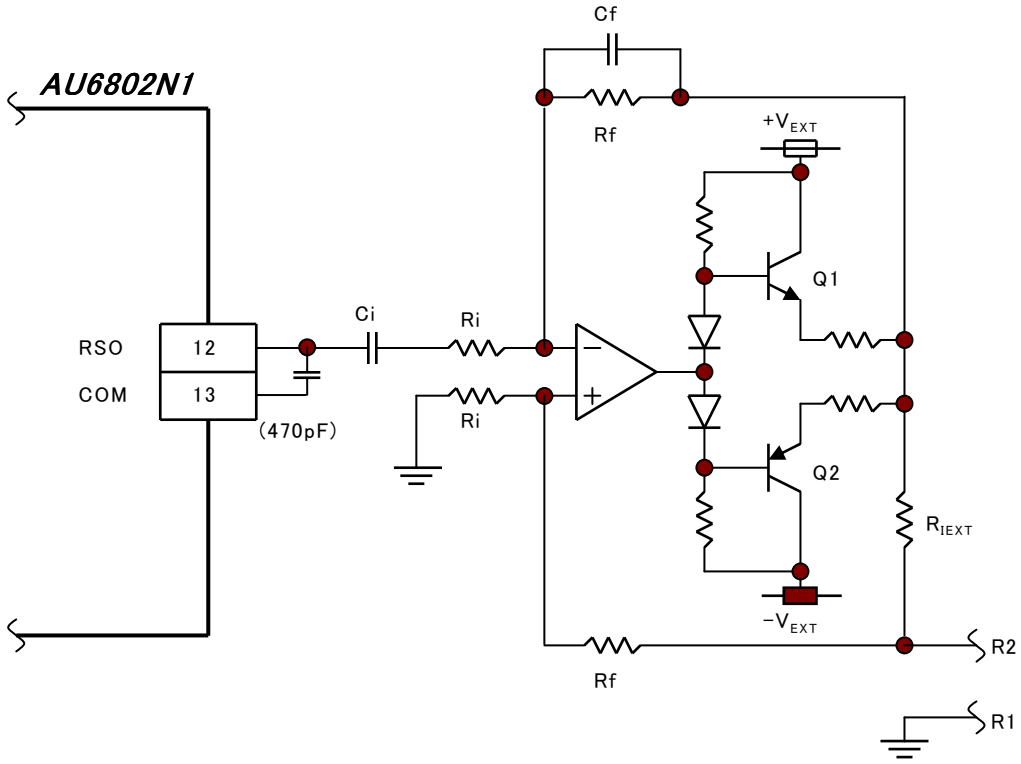
※ RSO output does not have enough driving power to excite resolver directly.

(1)Example circuit for single power source



In case of V_{EXT} variation is expected by battery power, possible minimum voltage must be considered as reference voltage.

(2)Example circuit for dual power source



■Method for setting constants

Refer below for setting constants.

≪Description of symbol≫

$+V_{EXT}$, $-V_{EXT}$: External power supply(For exciting voltage booster amplifier circuit)
I_{REF} : Exciting current of Resolver
R_{IEXT} : Resistor for setting exciting current of Resolver
V_{REF} : Exciting voltage of Resolver
Z_{RO} : Input impedance of Resolver(Specified value)
V_{RSO} : RSO pin (AU6802N1)output voltage (=2Vp-p typ.)

Step① : Calculate the exciting current by setting the exciting voltage based on the voltage of external power supply.

$$V_{REF} = I_{REF} \times Z_{RO}$$

Step② : Calculate the circuit constants based on the exciting current.

$$I_{REF}/2 = (V_{RSO} \times Rf) / (R_{IEXT} \times Ri) \quad \cdots\cdots \text{For single power source}$$

$$I_{REF} = (V_{RSO} \times Rf) / (R_{IEXT} \times Ri) \quad \cdots\cdots \text{For dual power source}$$

< Setting condition>

- $R_{IEXT} \leqq (Z_{RO} / 10)$ [Ω]
- $Rf \geqq 50k\Omega$, $Ci \times Ri \geqq 5 \times 10^{-4}$ [s] , $Cf \times Rf \leqq 5 \times 10^{-6}$ [s]
- The power supply for an operational amplifier should be the same as that for the transistor buffer.

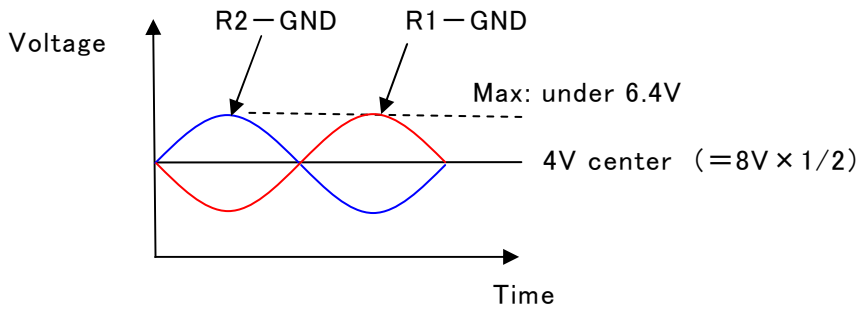
※Calculation method describing in specification is based on DC circuit concept.
Resolver is a AC circuit and that input impedance(= R(RESISTANCE) +jX(CONDUCTOR)) cause voltage phase shift and current phase shift. Also there are some impacts at parallel connection of Rf and Cf. Then it might not get exact exciting voltage value as calculated.
In such a case, please adjust each constant by yourself. (Voltage can be adjusted by R_i value.)
And it is effective to make pre-validation using circuit simulation like SPICE.

【Example】

Vext＝Battery 12V(8V～16V fluctuation), Excitation frequency＝10KHz,
Resolver Spec [Input impedance＝76Ω (R-part:18Ω＋L-part:1.18mH)]
Let's excite this resolver with current type amplifier described in P14.

Vext define as 8V(use minimum fluctuation).
Saturation voltage of OP-AMP assume as x0.8 supply. → 8V×0.8＝6.4V

Regarding R1-GND and R2-GND,
Set amplitude center as 4V (＝8V×1/2).
Set amplitude as 4Vp-p.
Then target amplitude is set as "R1-R2＝8Vp-p".



According to the formula of P15,

Resolver excitation current(I_{REF})＝0.11Ap-p (＝8Vp-p/76Ω)

R_{IEXT}＝4.7Ω ＜ Resolver input impedance(76Ω)/10
Rf＝100K
Then,

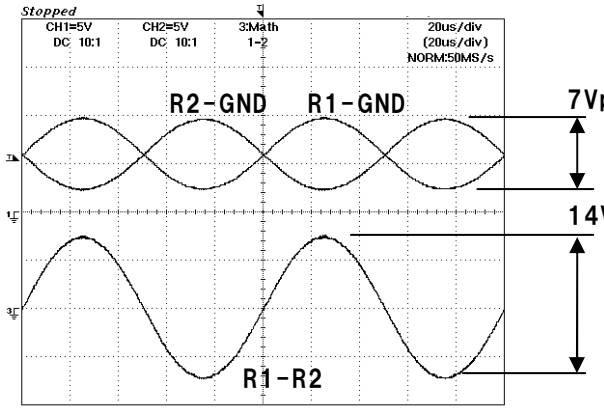
$$I_{REF} = \frac{V_{RSO} \times Rf}{R_{IEXT} \times Ri \times 1/2}$$

$$Ri = \frac{V_{RSO} \times Rf}{R_{IEXT} \times I_{REF} \times 1/2} = \frac{2Vp\text{-}p \times 100K}{4.7 \times 0.11 \times 1/2}$$

＝774K <----> (Please adjust at actual circuit.)

Example of circuit simulation,
Resolver input impedance ＝18Ω＋1.18mH
Cf ＝100p、
Emitter resistance ＝4.7Ω
Bias resistance ＝1KΩ
Then around Ri＝460KΩ. (8Vp-p between R1-R2)

【Single power source, V_{EXT}＝12V Waveform sample】

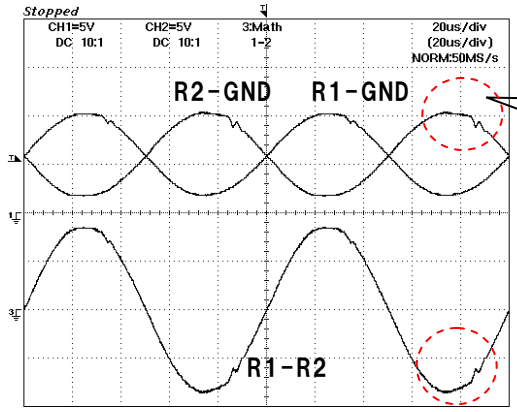


7Vp-p

6V center （＝1/2･V_{EXT}）

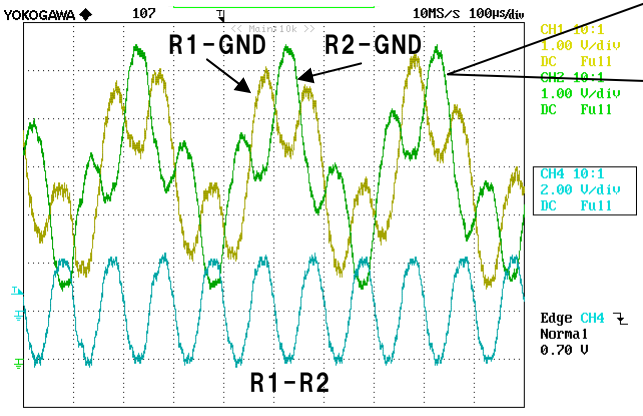
14Vp-p

0V center

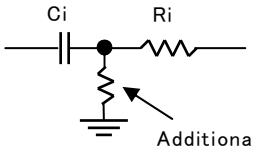


The wrong constant selection cause wider amplitude, and waveform distortion will be occurred by OP-AMP or Tr saturation voltage, etc.
Need to avoid distortion.

Rail to Rail OP-AMP type can set more wider active output voltage without distortion generation.



It might happen to have R1-GND/R2-GND oscillation due to OP-AMP characteristic.
If this kind of wave is observed, DC cut Capacitor(Ci)might cause unstability of DC current, then insertion of resistor between Ci output and GND will be effective to stabilize it.



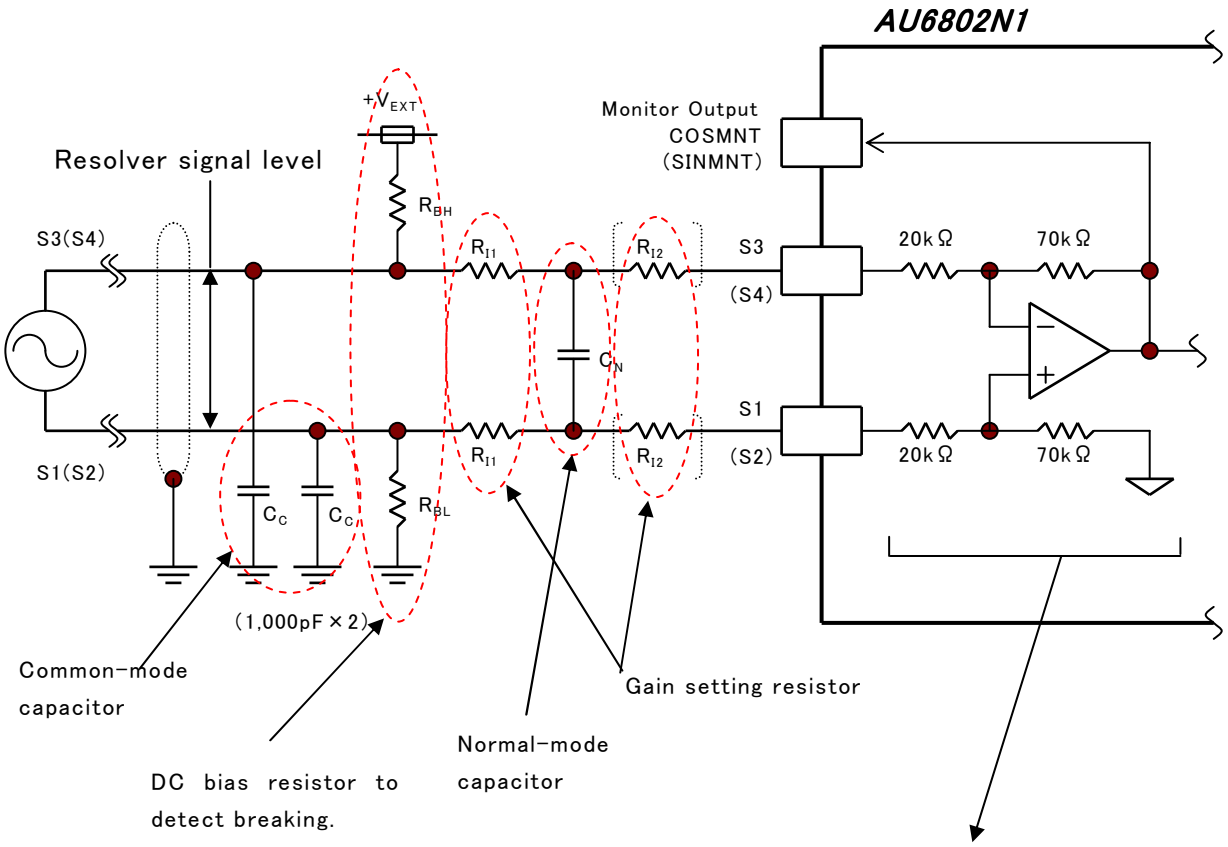
Additional resistor
（around 100KΩ）

4.2.2 Resolver Signal Input Circuit

R/D conversion of AU6802N1 will be done with monitor output(SINMNT, COSMNT). While voltage level of resolver signal is different with each application, it needs to set appropriate monitor signal level with gain adjustment of resolver input signal to fit R/D conversion effectively. Also it need to have external DC bias resistor activating the function which detect any breaking of Resolver signal lines (S1~S4) mounted in AU6802N1 devise.

In this chapter, show you example of resolver signal input circuit.

■**Example of resolver signal input circuit**



Specification of Differential Amplifier

	Min.	Typ.	Max.	Unit
Input Resistance	13	20	27	kΩ
Resistance ratio	0.99	1	1.01	—
Gain	3.47	3.5	3.53	—

(1) Gain setting resistor

R_I(=R_{I1}＋R_{I2}) value is defined to put in MAX range 2～3Vp-p of monitor output.

Monitor amplitude[Vp-p]＝Resolver signal amplitude[Vp-p]× $\frac{70K}{R_I+20K}$ while R_I＝R_{I1}＋R_{I2}

【Example】

Resolver spec(Exciting voltage: AC7Vrms, transformer ratio:0.286),
Use it as exciting voltage 10Vp-p, monitor output max amplitude assumed 2.5Vp-p.

Resolver output max＝2.86Vp-p （＝10Vp-p×0.286） then,

2.5[Vp-p]＝2.86Vp-p [Vp-p]× $\frac{70K}{R_I+20K}$ ∴R_I＝60K

In this case, due to the resistor value variability of AU6802N1 differential amplifier, monitor output max amplitude can be the range described in below table.

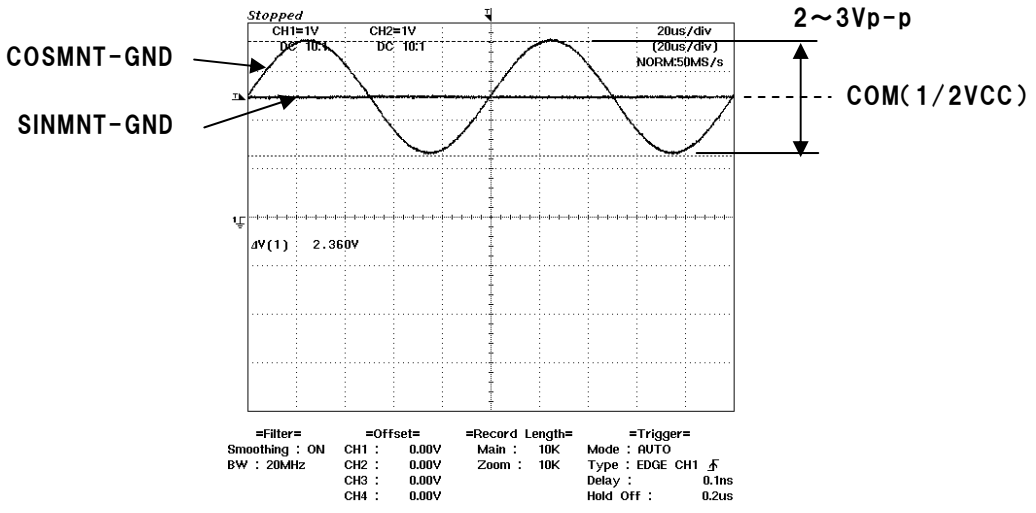
A range of monitor signal

	Min.	Typ.	Max.	Unit
Input R.	13	20	27	kΩ
Gain	3.47	3.5	3.53	—
Monitor signal	1.76 $(2.86\times\frac{13\times3.47}{60+13})$	2.5 $(2.86\times\frac{20\times3.5}{60+20})$	3.13 $(2.86\times\frac{27\times3.53}{60+27})$	Vp-p

Moreover, a range of monitor signal max amplitude will be varied by the deviation of resolver, transformation ratio and the deviation of input impedance.

※ In case of exceeding the max range(0.5～3.5Vp-p) of monitor signal amplitude, it cause to detect abnormal sensor signal.

Example of monitor waveform （At 0° ）



※If potential difference between SINMNT and CONMNT generate by the deviation of R_I, it cause a error source.
Please select appropriate resistor grade according to your system tolerance.

[Example] In case of there is a ＋Δ COSMNT against a SINMNT,

$$\text{Error} = -\frac{1}{2} \cdot \Delta \cdot \text{SIN}2\theta \quad [\text{rad}]$$

(Voltage difference 1% case: Δ＝0.01 then Error max＝±0.29° (＝±0.01/2 rad))

(2)DC bias resistor to detect breaking (R_{BH}、R_{BL})

When the signal line come down, monitor output level must be below the fault detecting level (0.15Vcc＝0.75V).

Without this bias resistor, fault detection depends on its angle.
(In fault case, If normal side monitor signal go under the fault detecting level, fault can detect as breaking of exciting source line.)

Estimated value of R_{BH}、R_{BL} is shown below with some V_{EXT} voltage.

VEXT	R_{BH}[KΩ]	R_{BL}[KΩ]
+5V	20	20
+12V	50	
+24V	100	

(3)Normal mode capacitor (C_N)

While basic circuit doesn't have C_N、it can improve electrical noise.

But gain resistor (R_{I1}) and C_N work as filter, it causes one of factor of phase shift.

Time constant＝2×(R_{I1}//(R_{i2}＋20K))×C_N

R_{i1}//(R_{i2}＋20K) means parallel connection of R_{i1} and (R_{i2}＋20K).

This capacitor has an impedance{＝1/(ω・C_N)} and it affect signal level also.
Deviation of capacitor is much worse than the deviation of resistor; please select the small deviation parts or small capacitance parts to avoid impact of signal level.

(4)Common mode capacitor (Cc)

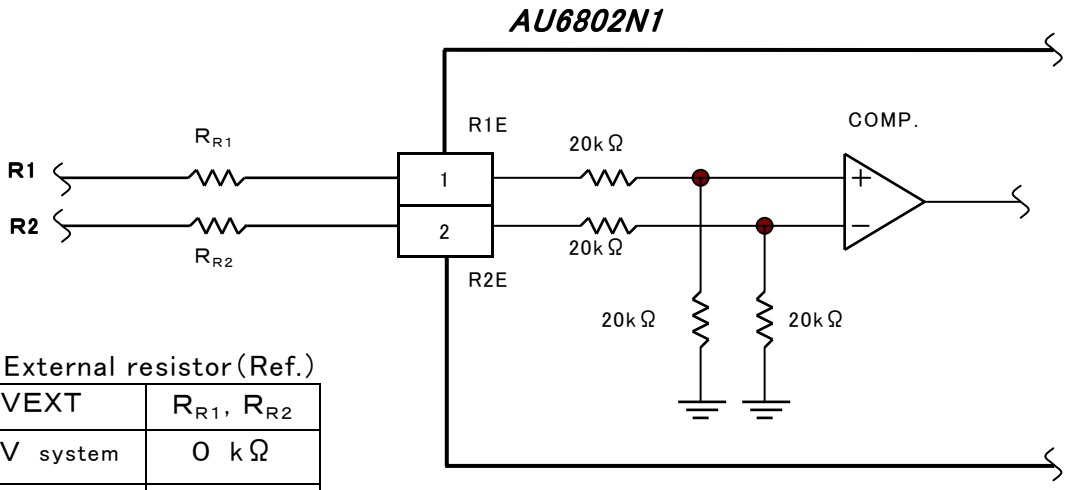
Standard usage is putting 1000p capacitance between S1~S4 signals and GND.

4.2.3 External Input Circuit for exciting the **Resolver**

AU6802N1 R/D conversion include synchronous detection function which use a phase signal with the external input (R1E、R2E) of resolver excitation signal. Then R1E/R2E terminals need to have same phase input signal with the carrier of resolver signal.

In this chapter, there shows example external input circuit of resolver excitation signal.

(1)Basic circuit sample (using single power source for exciting amplifier)

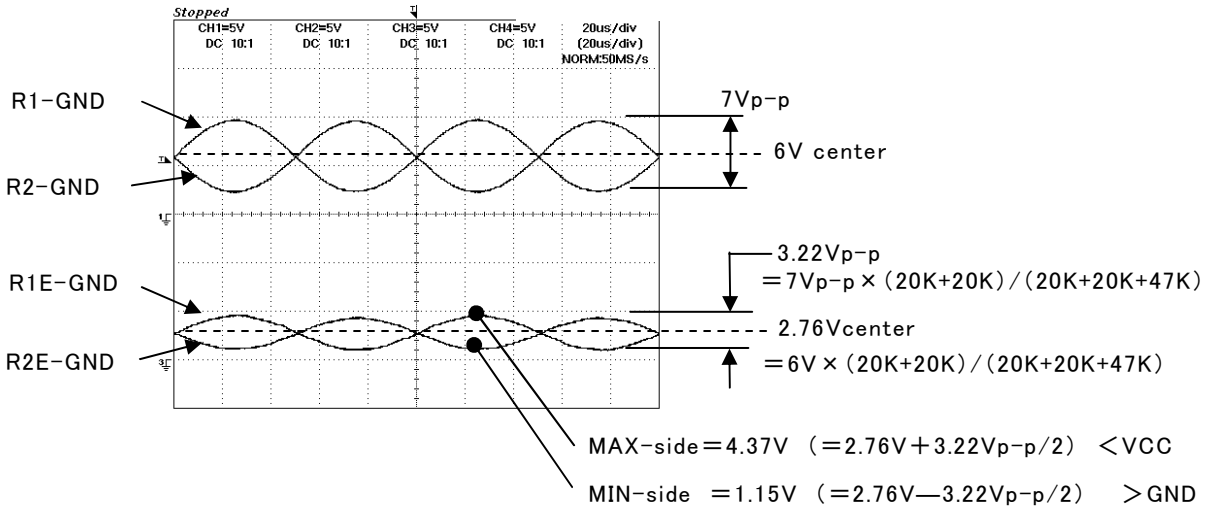


External resistor(Ref.)

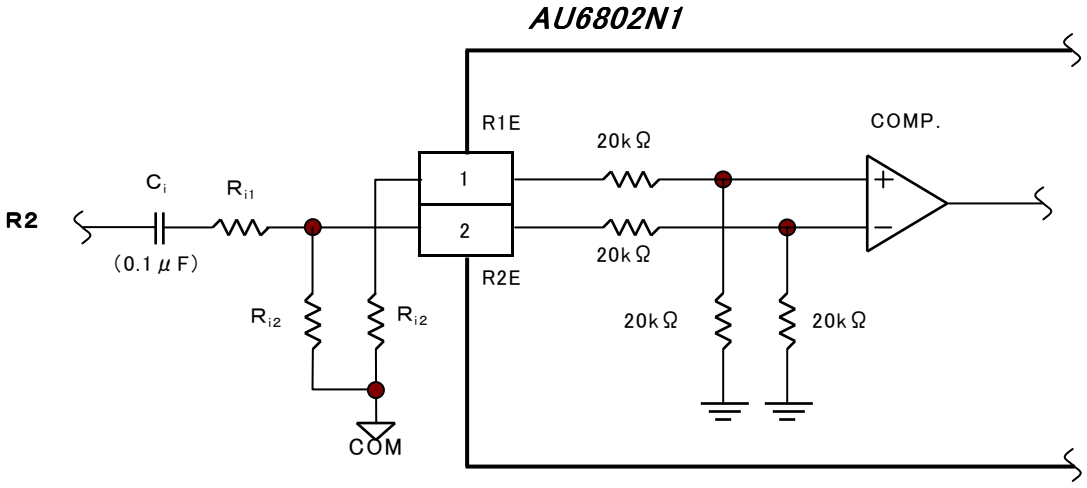
VEXT	R_{R1}, R_{R2}
+5V system	0 kΩ
+12V system	47 kΩ
+24V system	120 kΩ

In case of direct input for R1E/R2E, exciting signal level might exceed VCC and it cause some failure. So please note that the terminal voltage for R1E/R2E should not exceed VCC(Power supply voltage) by means of adding the external resistor(R_{R1}、R_{R2})to divide the voltage.

R_{R1}, R_{R2}＝47KΩ example



(2)Basic circuit sample (using dual power source for exciting amplifier)



In this dual power source case, an exciting signal is 0V center. So it needs to make R1E/R2E terminal input level as shifting DC level. There might happen to exceed 0V~VCC range of R2E terminal voltage, and it cause some failure. Then the terminal voltage for R2E should not exceed 0V~VCC by means of adding the external resistor(R_{i1}、R_{i2})to divide the voltage.

DC cut Capacitor(Ci)＞0.1μ

R_{i2}= around 3.3～4.7KΩ　（ around 10% of （20KΩ＋20KΩ） ）

Center value of swing [V] ＝COM [V]×$\dfrac{20K+20K}{20K+20K+R_{i2}}$

Amplitude level [Vp-p] ＝R2 [Vp-p]×$\dfrac{R_{i2}}{R_{i1}+R_{i2}}$

Waveform max value＝(Center of swing)＋(Amplitude level)/2 ＜ VCC

Waveform min value＝(Center of swing)－(Amplitude level)/2 ＞ 0V

COM current＝$\dfrac{COM-R2\min}{R_{i1}+R_{i2}}$ ＜ 2mA

【例】

Assuming R2＝10Vp-p.

And also assuming R_{i2}＝4.7K.

Center value of swing＝2.5V×$\dfrac{20K+20K}{20K+20K+4.7K}$＝2.24V

Assuming 3Vp-p for R2E amplitude level.

3 [Vp-p]＝10 [Vp-p]×$\dfrac{4.7K}{R_{i1}+4.7K}$　∴R_{i1}＝10.9K→11K

Waveform max value＝2.24V+3V/2=3.74V ＜VCC “OK”

Waveform min value＝2.24V－3V/2=0.74V ＞0V “OK”

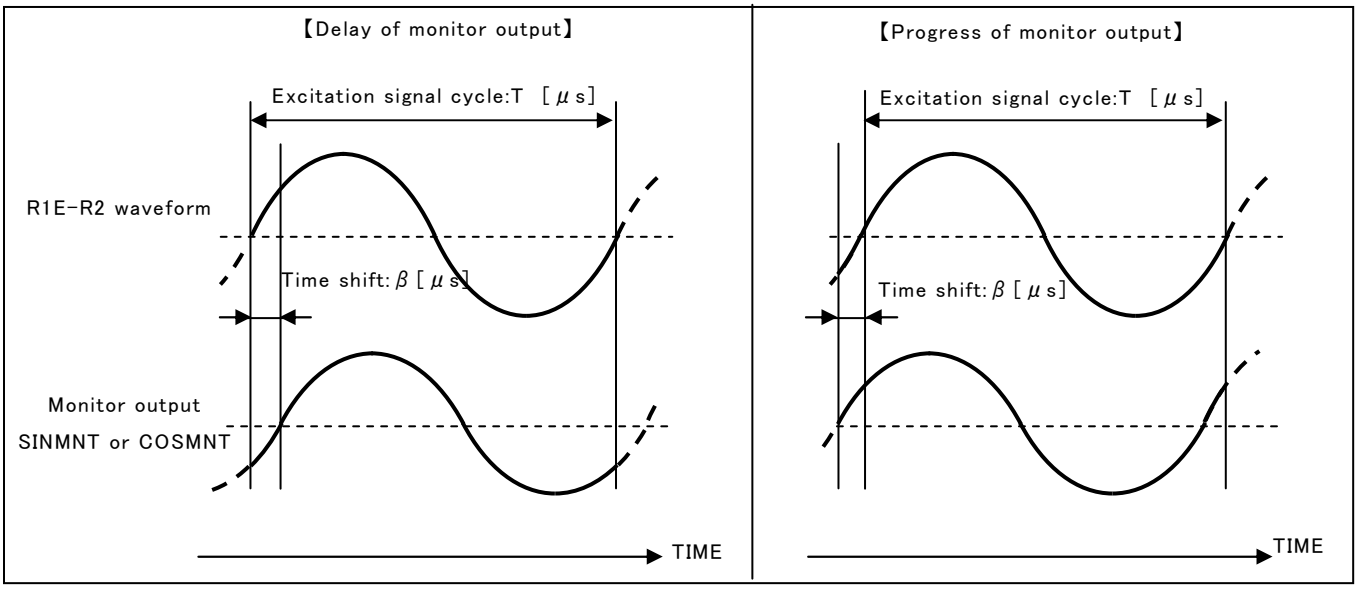
COM current＝[2.5V－(－5V)]/(11K＋4.7K)＝0.48mA ＜ 2mA “OK”

(3)Considering the phase shift

When any phase difference exists between the exciting component of Resolver signals (S1-S3, & S2-S4) and the external input signal for exciting Resolver (R1E/R2E), the loop gain of R/D conversion loop is equivalently decreased, which may affect the performance of R/D conversion. That means that it spent long time to settle down the angle output or not be able to settle down the angle data.

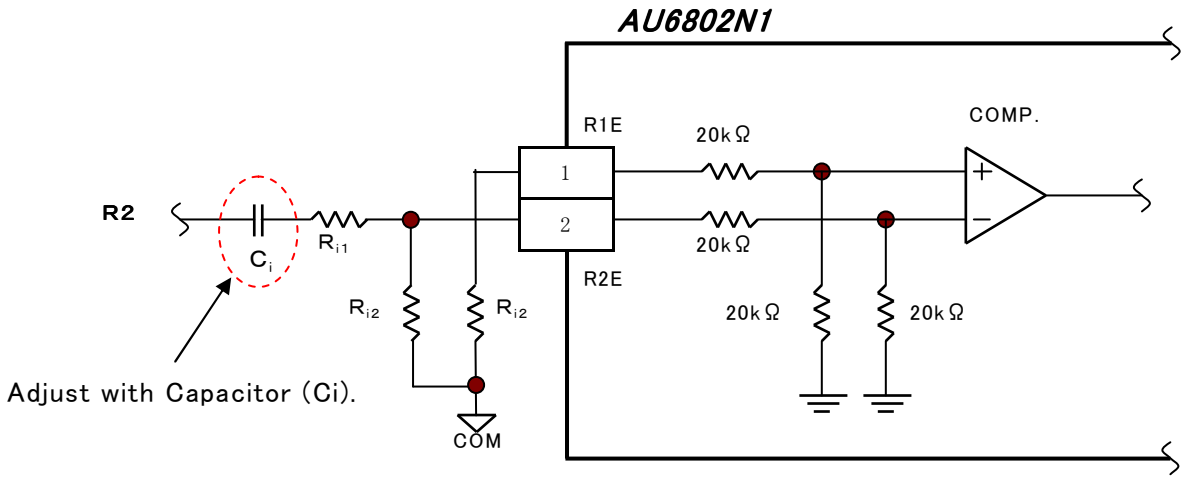
In case of phase shift existing, a phase adjustment circuit should be inserted into the R1E/R2E line so that the phase difference is 10 degree or less. As confirmation, the phase shift may be adjusted between the exciting component of Resolver signal monitor terminals (COSMNT & SINMNT) and the external input signal for exciting Resolver (R1E/R2E).

■ How to convert an angle from phase shift.



$$\text{Phase shift angle}(\alpha)\text{corresponding value}(^\circ) = \frac{\beta}{T} \times 360^\circ$$

①How to adjust progressing phase



There might happen to exceed 0V~VCC range of R2E terminal voltage, and it cause some failure. Then the terminal voltage for R2E should not exceed 0V~VCC by means of adding the external resistor(R_{i1}、R_{i2})to divide the voltage.

■The amount of progressing phase(indication)

"The amount of progressing phase" $\alpha = \arctan\left\{\dfrac{1}{2\pi \times f \times C_i \times (R_{i1} + R_{i2})}\right\}$ [degree]

【Example】
When R2＝10Vp-p, would like to set 10° for progressing phase.
(excitation frequency＝10KHz)

※ R_{i1}、R_{i2} concept is same as chapter 4.2.3(2) .

Assuming R_{i1}＝11K、R_{i2}＝4.7K ,

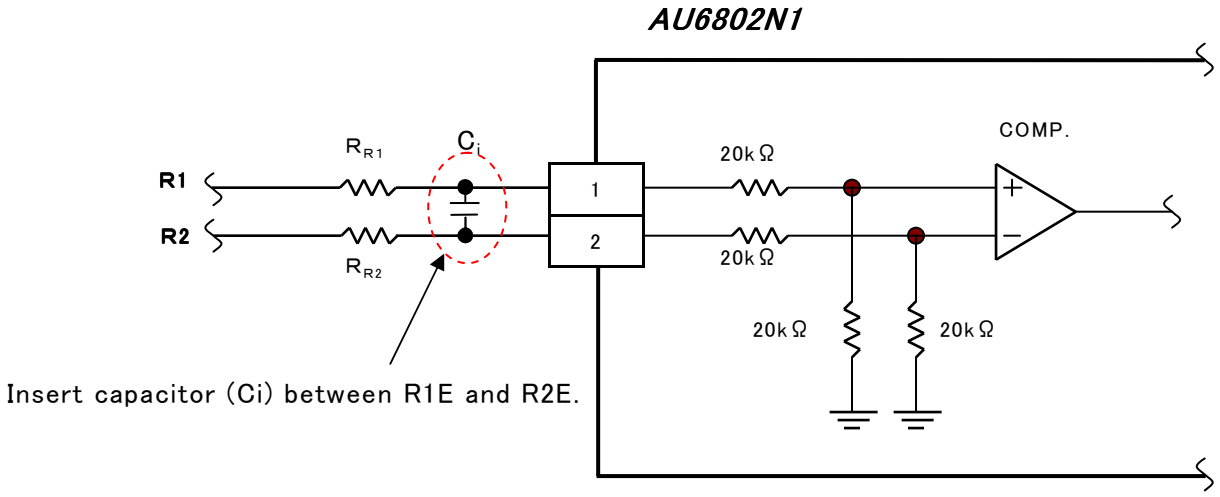
$$10° = \arctan\left\{\frac{1}{2\pi \times 10000 \times C_i \times (11K + 4.7K)}\right\}$$

$$C_i = \frac{1}{2\pi \times 10000 \times (11K + 4.7K) \times \tan 10°}$$

＝0.00575 μ → 0.0056 μ
(Please adjust it with actual circuit.)

②How to adjust delaying phase

②-1 Basic circuit to adjust delaying phase
(Use single power source for exciting amplifier)



■The amount of delaying phase(indication)

"The amount of delaying phase" $\alpha = \arctan[2\pi \times f \times C_i \times 2 \times (R_{R1} // (20K + 20K))]$ [degree]

"R_{R1}//(20K＋20K)" means parallel connection resistor value of R_{R1} and (20K＋20K).

【Example】
When R_{R1}、R_{R2}＝47K, would like to set 10° for delaying phase.
(excitation frequency＝10KHz)

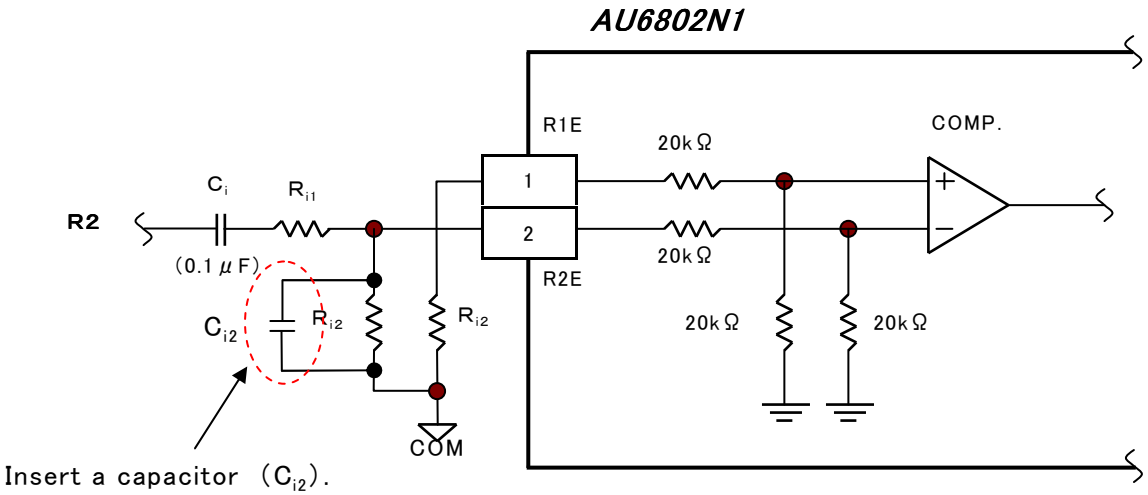
R_{R1}//(20K＋20K)＝21.6KΩ

$$10° = \arctan(2\pi \times 10000 \times C_i \times 2 \times 21.6K)$$

$$C_i = \frac{\tan 10°}{2\pi \times 10000 \times 2 \times 21.6K}$$

＝65p → 68p
(Please adjust it with actual circuit.)

②-2 Basic circuit to adjust delaying phase (using dual power source for exciting amplifier)



■The amount of delaying phase(indication)

"The amount of delaying phase" $\alpha = \arctan[2\pi \times f \times C_{i2} \times (R_{i1} // R_{i2})]$ [degree]

$(R_{i1} // R_{i2})$ means parallel connection resistor value of R_{i1} and R_{i2}.

【Example】
When R2＝10Vp-p, would like to set 10° for delaying phase.
(excitation frequency＝10KHz)

※R_{i1}、R_{i2} concept is same as chapter 4.2.3(2) .

Assuming R_{i1}＝11K, R_{i2}＝4.7K,

Then $R_{i1} // R_{i2}$＝3.3KΩ

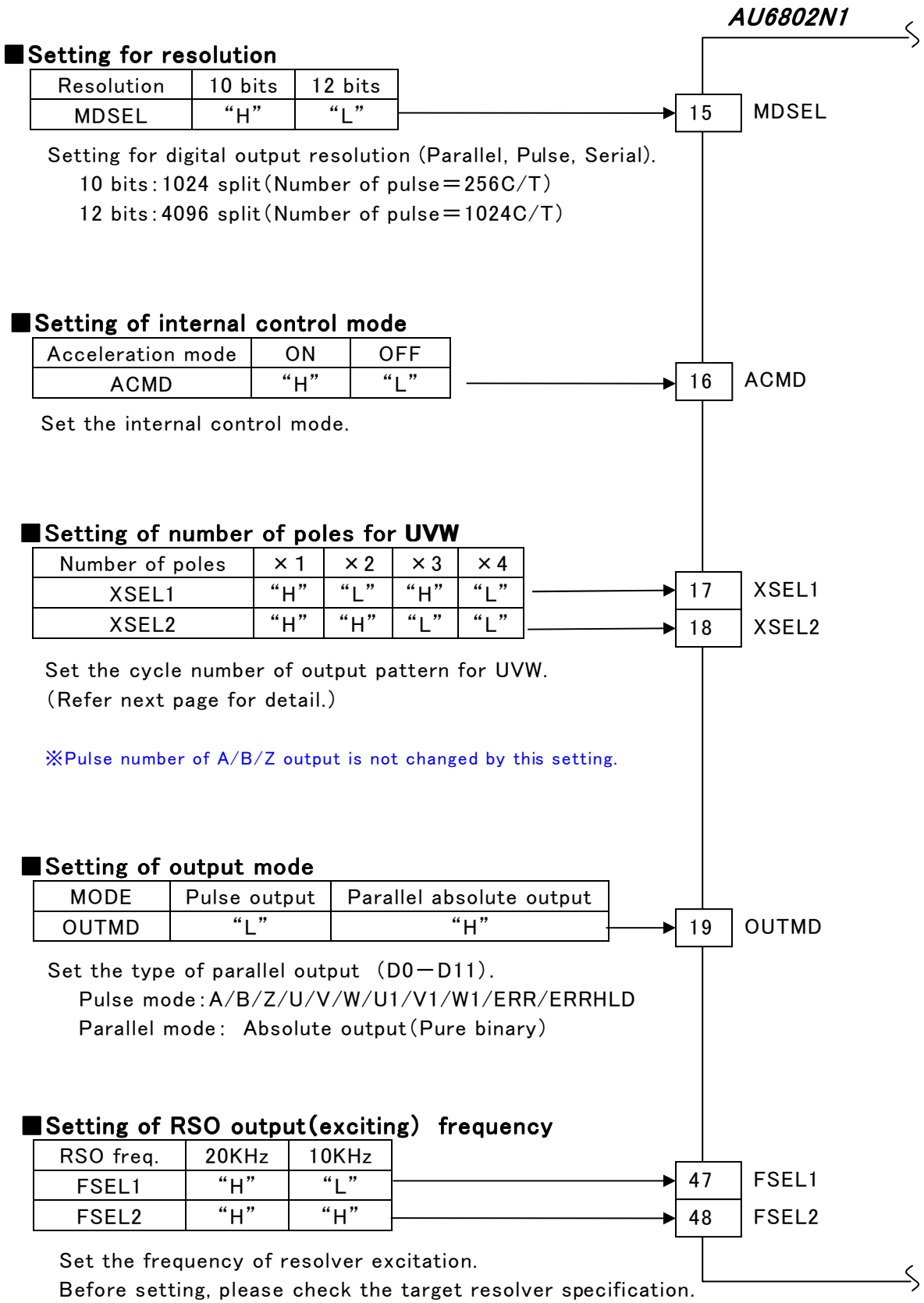
$$10 = \arctan(2\pi \times 10000 \times C_{i2} \times 3.3K)$$

$$C_{i2} = \frac{\tan 10°}{2\pi \times 10000 \times 3.3K}$$

＝850p → 910p
(Please adjust it with actual circuit.)

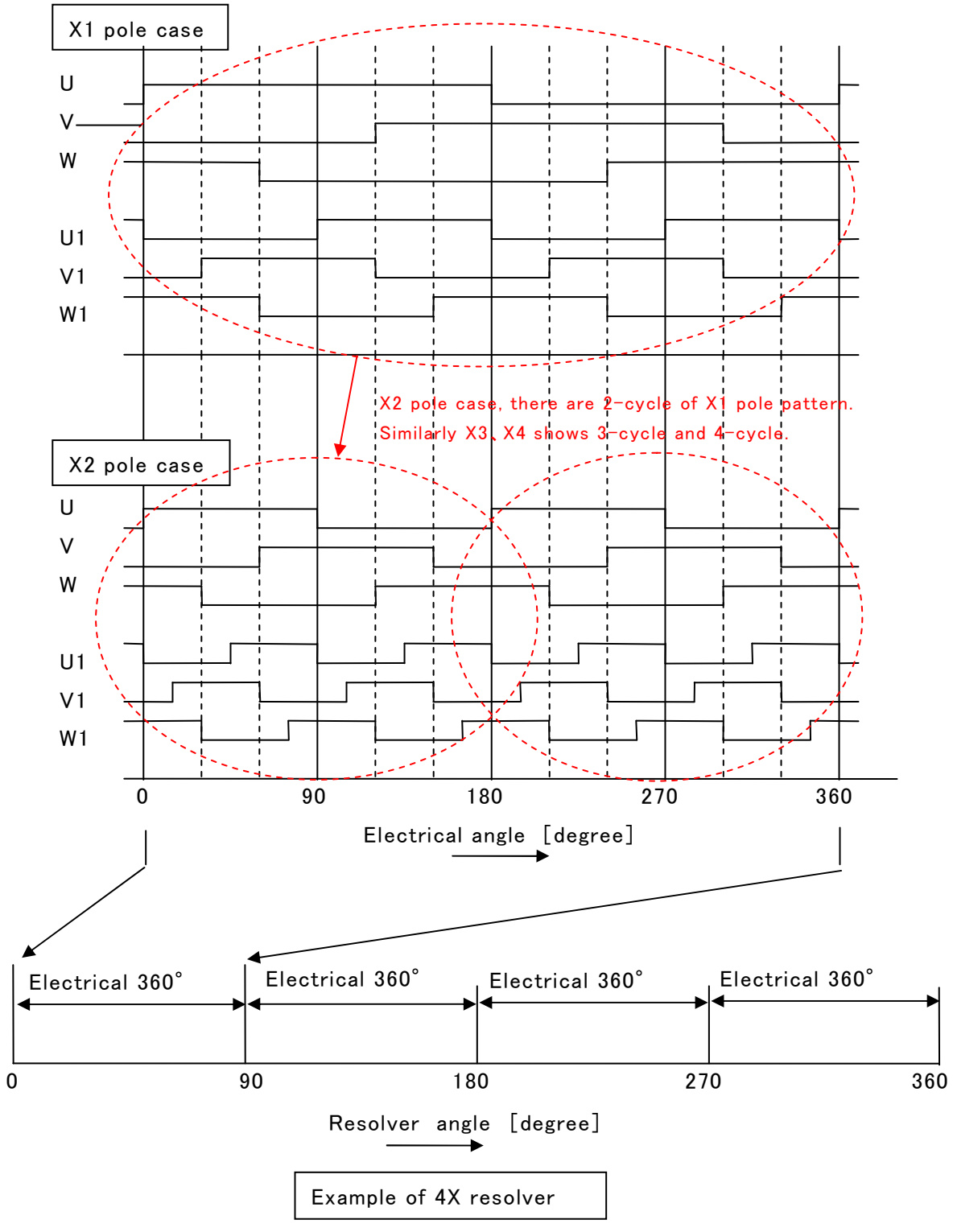
4.3 Digital Interface

4.3.1 System Setting



■Setting number of poles of UVW

※ This specific setting(X1, X2, X3, X4) means cycle number of waveform output pattern which range is 0~360 degree of electrical angle. It does not have any relation with resolver multiplication factor of angle (X1, X2, X3, X4).



Example of 4X resolver

【Example】

In case of 8 poles（4 pole pair） motor, the relationship of resolver multiplication factor and the setting number of poles for UVW is below.

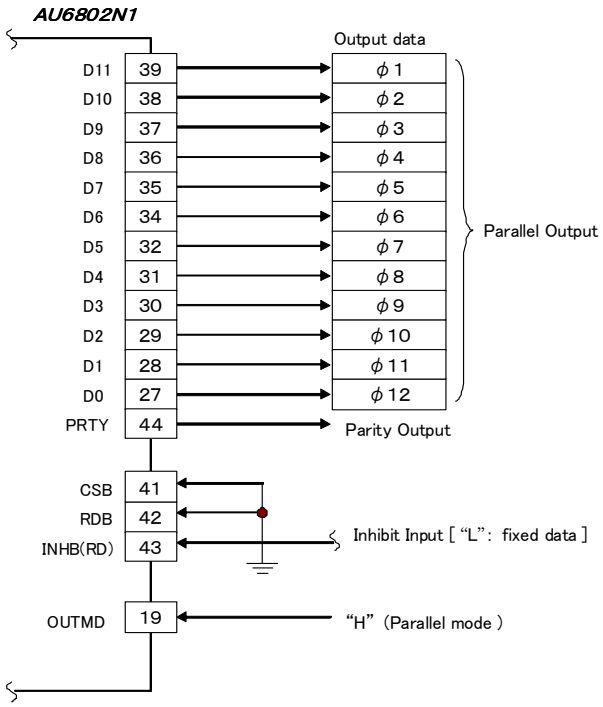
Resolver X数	UVW poles
4X	×1
2X	×2
1X	×4

Each combination output 4 pulse of UVW (every 90 degree) while one revolution of Resolver.

4.3.2 Output Interface

(1)Parallel Output mode (Parallel output is set by OUTMD＝“H”.)

■Parallel I/O interface mode《Stand-alone》 : Interfaced by dedicated I/O

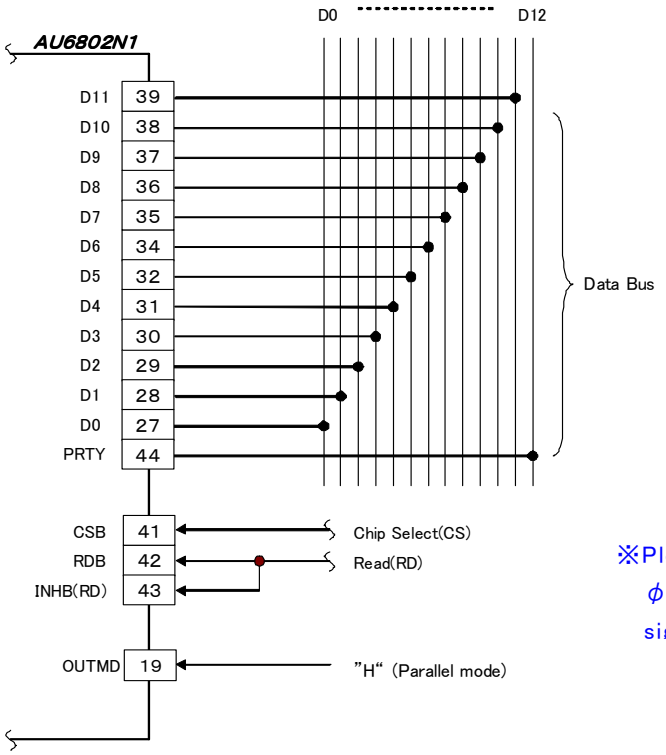


CSB＝“L”
RDB＝“L”
Data can read with controlling “INHB”

Refer to SPEC p17 (Figure-14).

※Please refer section-9.8 for φ1～φ11、PRTY、INHB signal timings.。

■Parallel BUS interface mode《Bus output》 : interfaced by BUS line

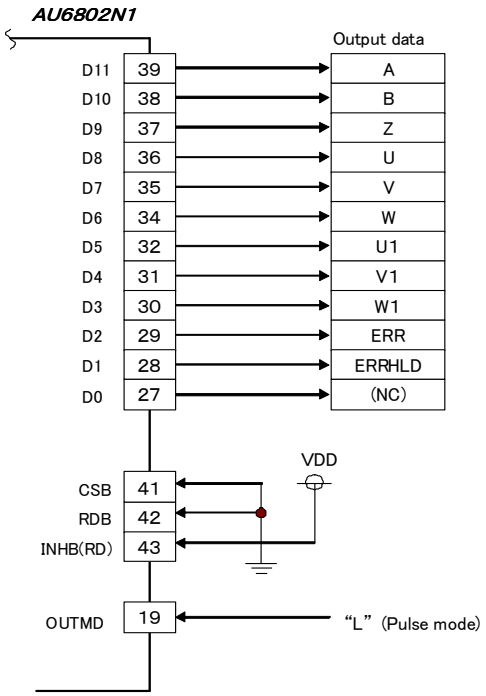


Data can read with controlling CSB、RDB (＝INHB).

Refer to SPEC p17 (Figure-13).

※Please refer section-9.8 for φ1～φ11、PRTY、CSB、RDB、INHB signal timings.。

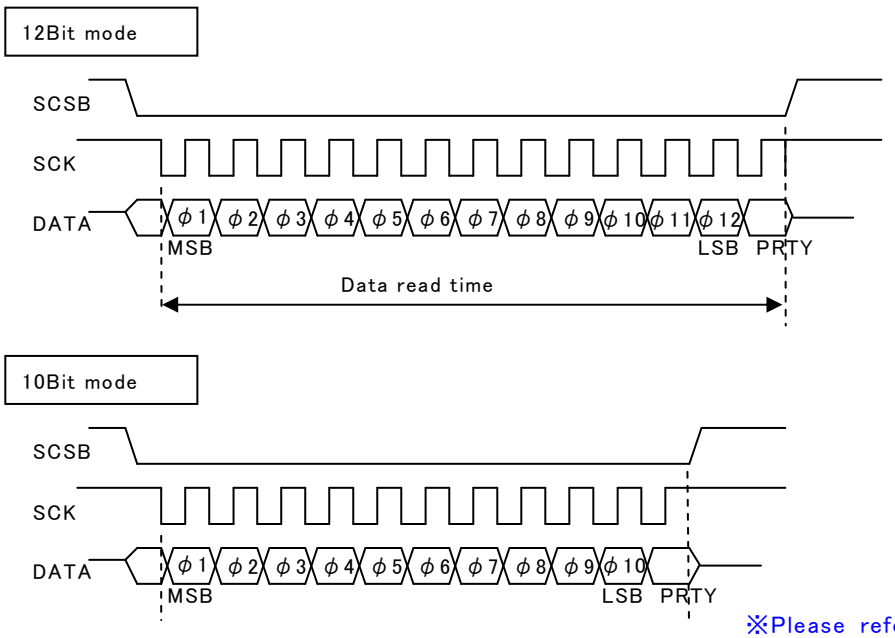
(2)Pulse interface mode （Pulse output mode is set by OUTMD＝“L”.）



Settings are below.
CSB＝“L”
RDB＝“L”
INHB＝“H”

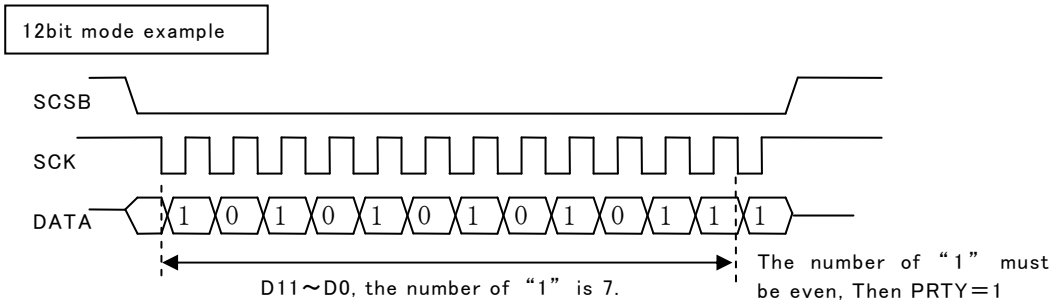
(3)Serial output mode

○Serial output data is controlled by “SCSB”、”SCK”.

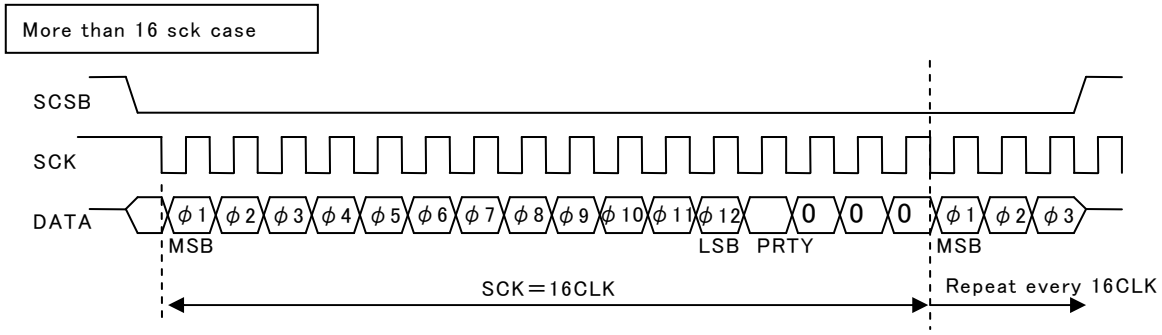


※Please refer section-9.8 for each signal timings.

○PRTY is defined as even parity. The number of “1” data between “φ1～φ12” and “PRTY” must be even.



○While SCSB＝“L” fix, output data repeat every SCK 16 clocks.
Then 14th ~16th data fix as “0”.



(4)Serial output mode ＋A/B pulse mode

The absolute angle detection is possible with serial out mode and A/B pulse mode. Power-up starting time, first absolute data read with serial output mode. Since then absolute data can count UP/DOWN with A/B pulse data. So you can reduce the number of CPU interface as 6 line (serial 3lines＋A/B/Z 3lines)

Combination usage of serial mode and parallel mode can be used for fail detection of digital output data.

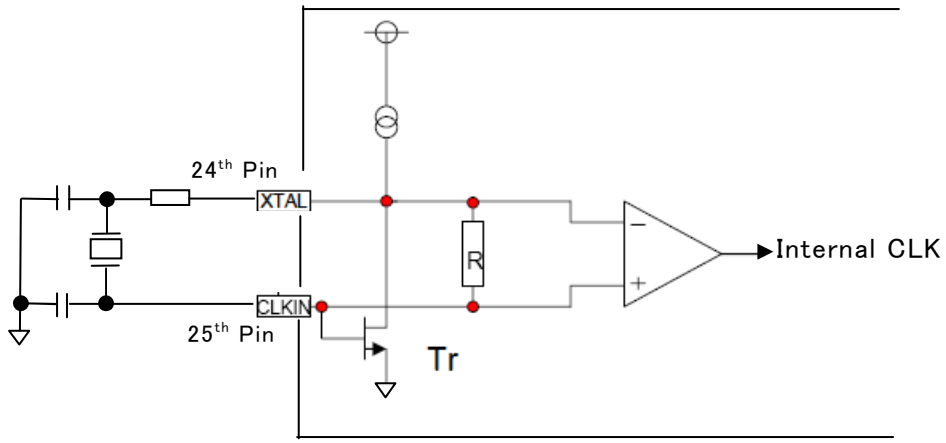
4.4 Clock Input(20MHz)

4.4.1 Crystal Resonator / Ceramic Resonator

Below describes equivalent circuit of resonator section. CLKIN is inverted signal of XTAL and these 2 pins connect to comparator input. While there is cross point between XTAL voltage and CLKIN voltage, internal CLK will be stable. In this case it is possible to use another devise which does not list in recommended parts documented in specification (P30, Figure25).

Each case you select resonator included in recommended one, we recommend you to ask resonator company about optimal constant oscillation of your actual print board. Cause there might change their oscillation condition due to wiring pattern difference.

AU6802N1 equivalent circuit of resonator section.

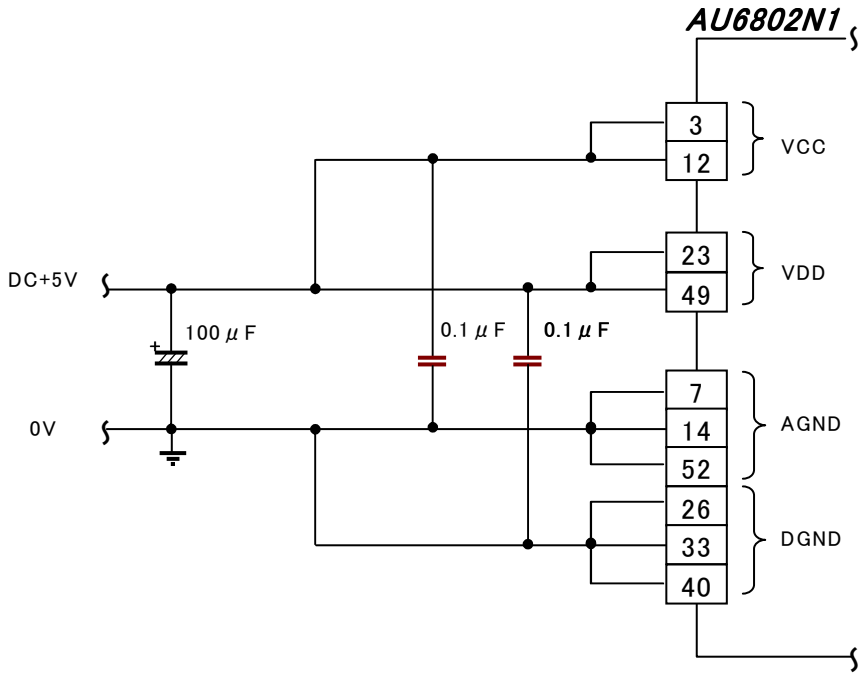


4.4.2 External Clock

In the case of external clock, clock must connect to CLKIN(25th Pin) and XTAL should be open (NC). CLKIN pin is TTL-level input.

※ 20MHz clock might be noise source.
It is effective for EMC countermeasure to make signal pattern wider and shorter, also guard by GND line.

4.5 Power Source



Power source is single supply +5V±5%. Analog power line and Digital power line can connect to same power line. If you set separate power line for analog(VCC) and digital(VDD), there must be no potential difference between VCC and VDD, or AGND and DGND. Also power switching (power-on or power-off) should be done simultaneously.

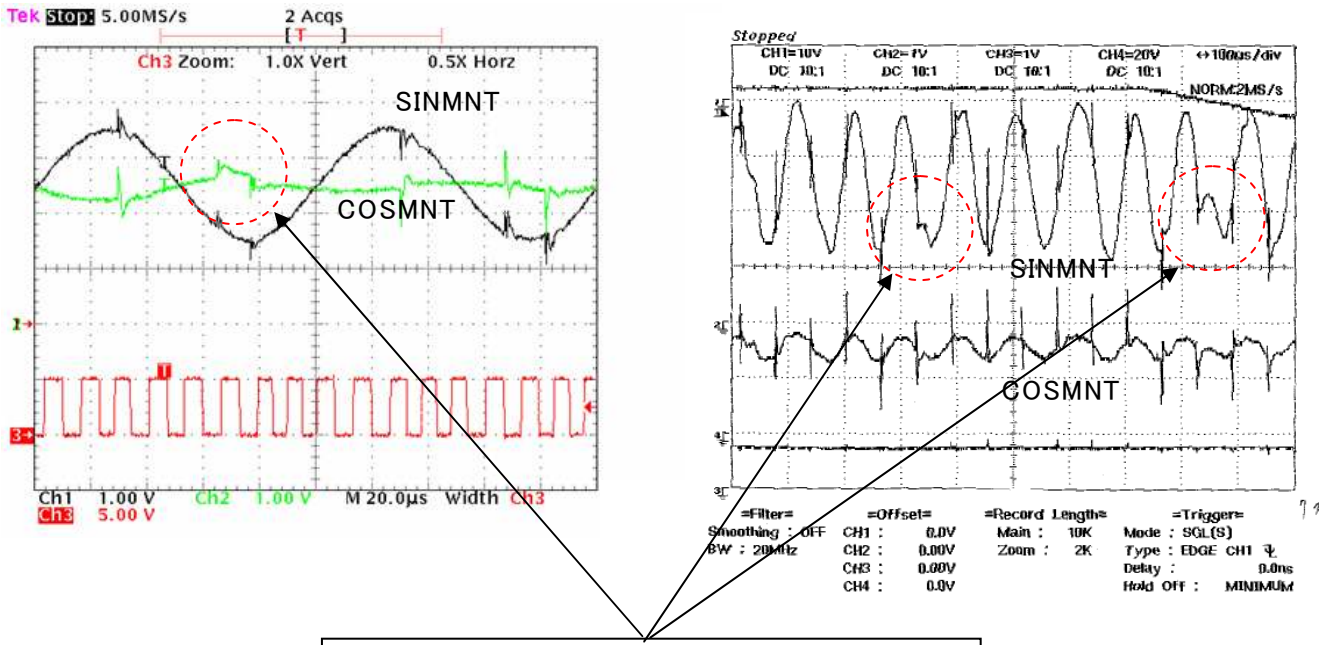
Above figure is example of power connection. No need to collect analog power line or digital power line. Regarding 0.1uF capacitors, it should be located close to AU6802N1 device as much as possible.

4.6 Countermeasures for Noise

Below waveforms are measured actually. Countermeasure for noise must be done in accordance with the specification P34 contents.

■Waveforms of magnetic noise

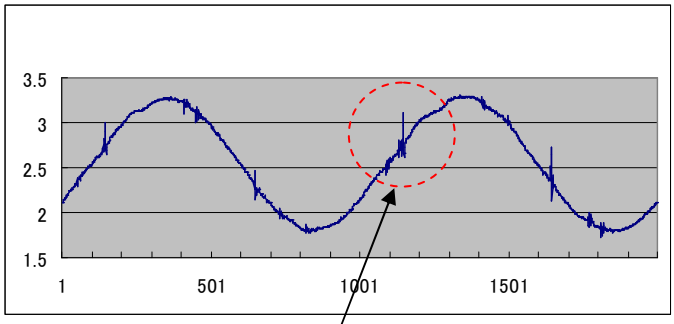
Magnetic noise happens when the leakage flux of the motor passes through the resolver. Its effect will be bigger turbulence of digital output, which will generate error.



Basic waveform(10KHz) deformed.

■Waveforms of electrical noise

Electrical noise happens when the spike noise caused by PWM drive of the motor affects signal lines. Turbulence of digital output will not be so big, but it will generate error depend on the size of noise.



Basic waveform(10KHz) was not changed much .
But spike noise was overlapped.

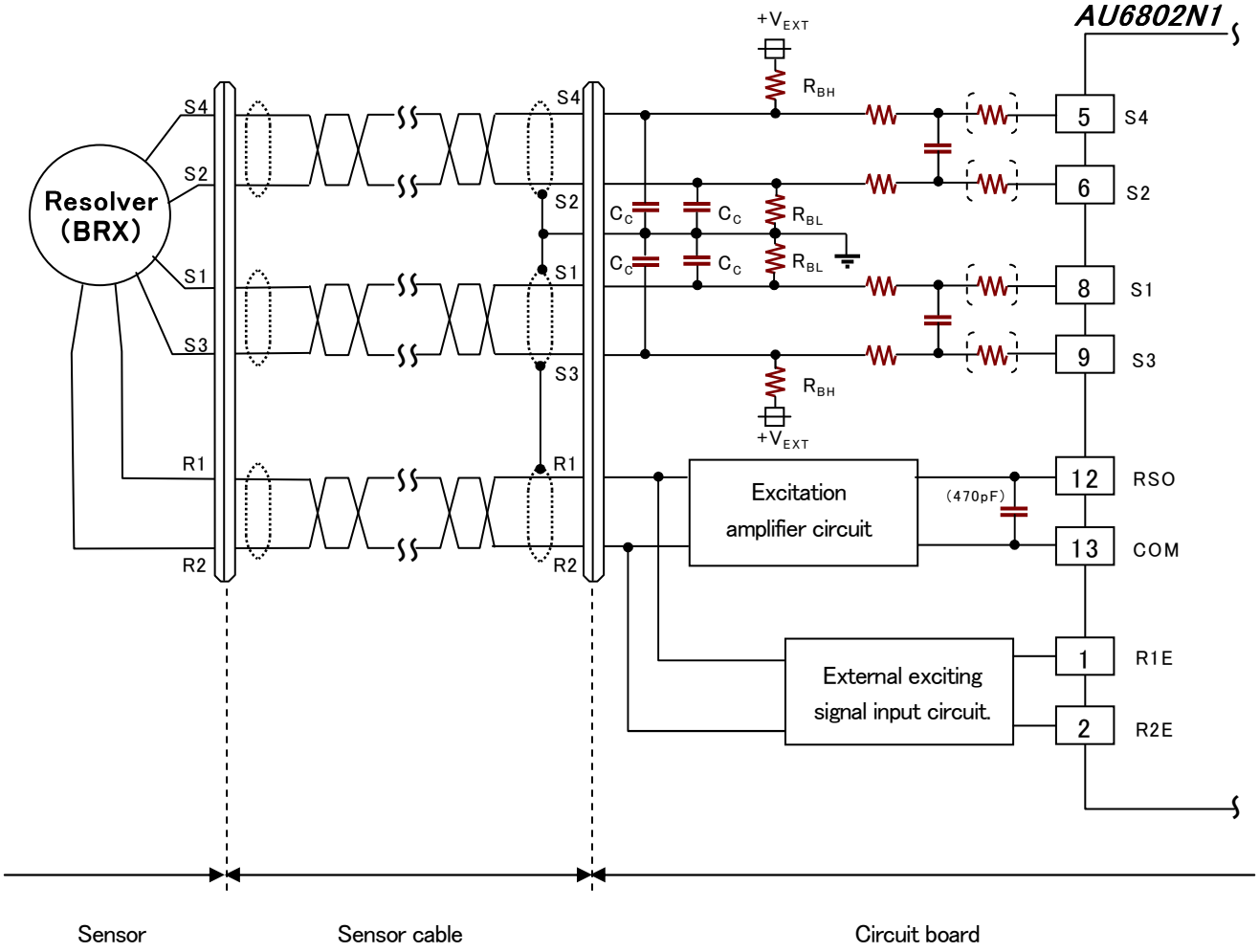
5. Connection

Caution !

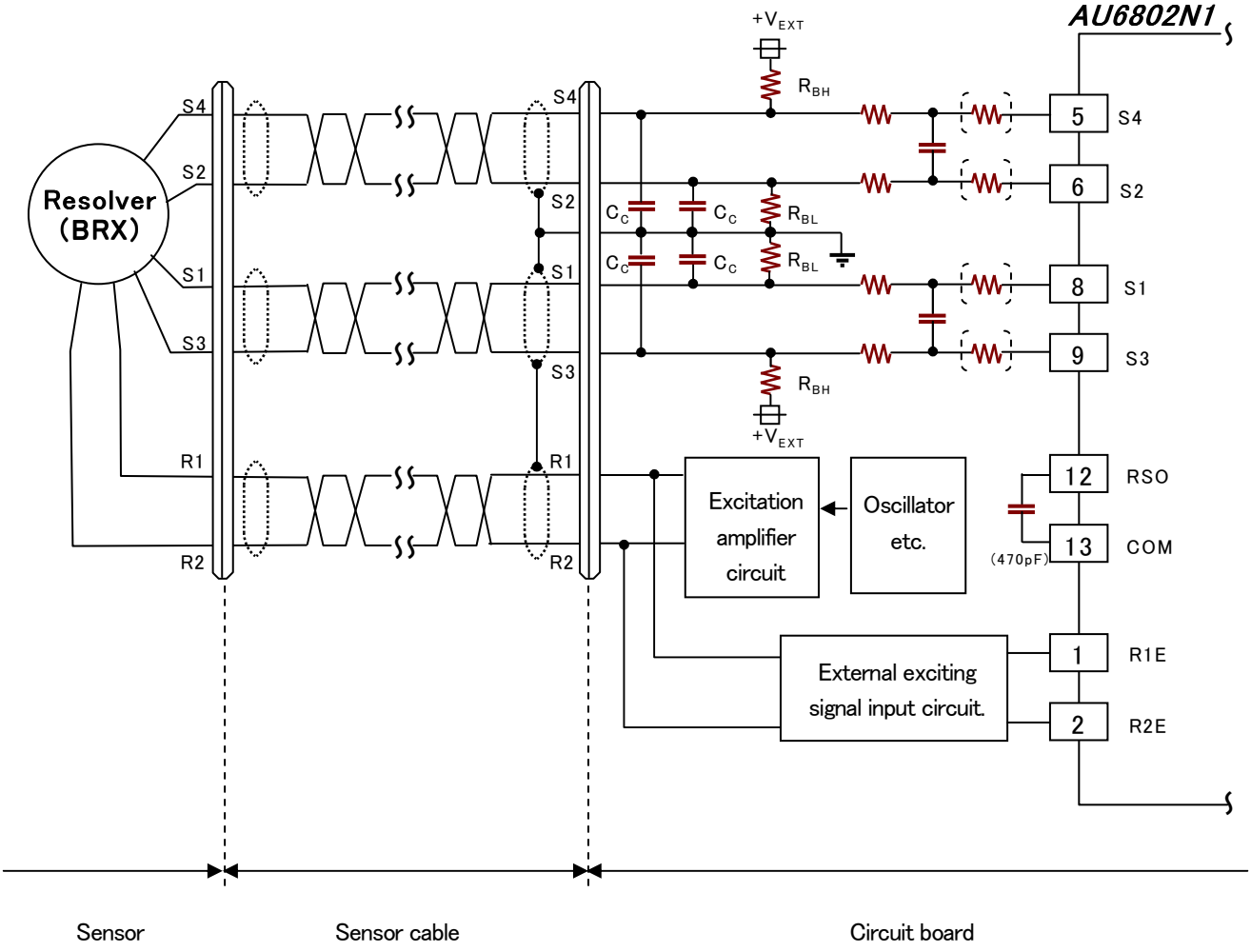
Please take off the power during connection operation. After power off, take enough time, check the voltage value by tester, then please operate wiring and connecting.

5.1 Example of Resolver Connection

■Connection example: Used “RSO” as excitation source.



■Connection example: Used external oscillator as excitation source.



Resolver output signals (S1、S2、S3、S4) are connected to each corresponding AU6802N1 terminals (S1,S2,S3,S4) through the resolver signal input circuit. Resolver input signals (R1,R2) are connected to each corresponding AU6802N1 terminals (R1E,R2E) through the external exciting signal input circuit. Regardless of whether RSO output use or not, there must be capacitor connection between RSO and COM.

5.2 Example of Power Connection

Refer the section 4.5

6. Check Point of Operation

Caution !

Before power-up, please make sure the connection which is no mistake.

6.1 Check Point for Resolver Interface

6.1.1 Check Point of Excitation Signal

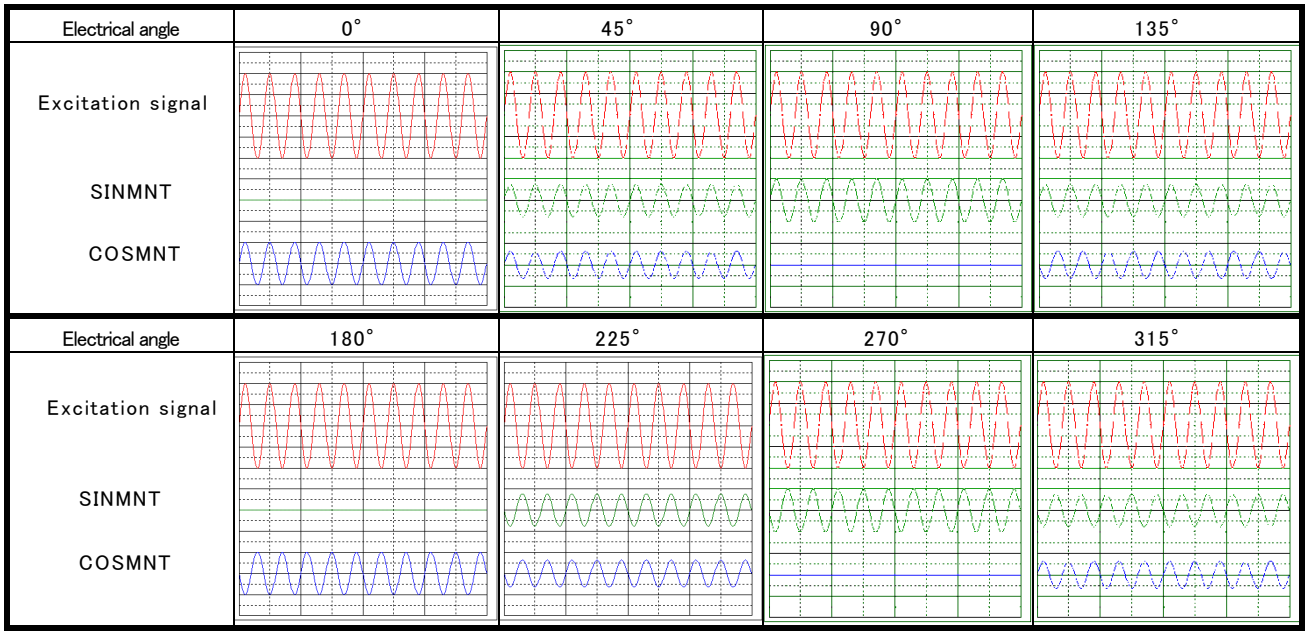
Check your resolver excitation signals(R1,R2) whether the resolver is excited with your designed amplitude or not. If signals are small or saturated situation, please review your excitation amplifier circuit again. If there are no signals, please check the connection to resolver and power supply status.

6.1.2 Check Point of Monitor Signal Amplitude

(1)Check point of amplitude change

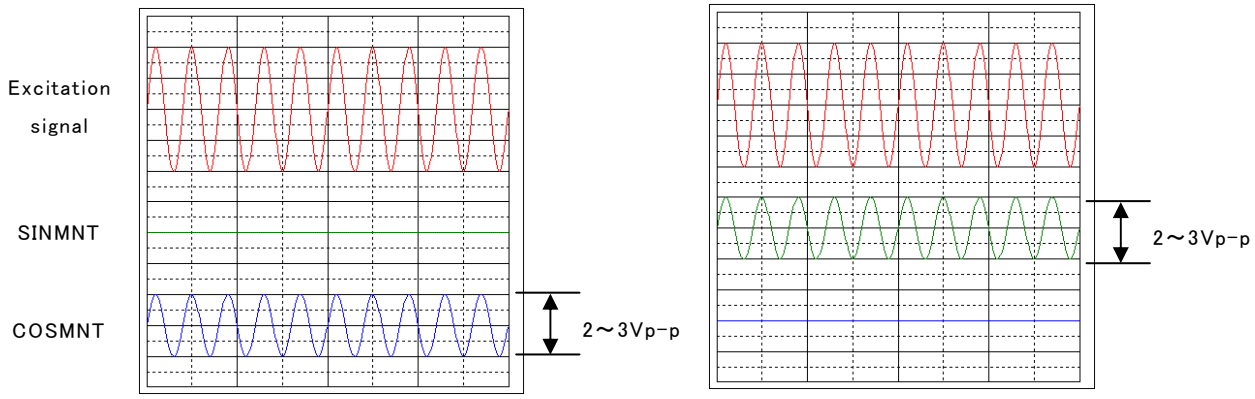
Observing the waveform of resolver exciting signals and monitor output (SINMNT、COSMNT), please check if the monitor output have a same frequency carrier of excitation signals. After then, rotate the resolver, please check that monitor signal amplitude is changing with corresponding resolver angle. If there is no signal or no amplitude change by rotation, please check the connection between resolver and AU6802N1.

■Waveform example of exciting signal and monitor signal with some fixed angle.



(2)Check point of amplitude level.

Rotating the resolver with observing a monitor signal, please check the monitor signal (SINMNT and COSMNT) maximum amplitude its recommended range is 2~3Vp-p. If signal amplitude is not appropriate range, please adjust your circuit constants of exciting amplifier and resolver signal input circuit.

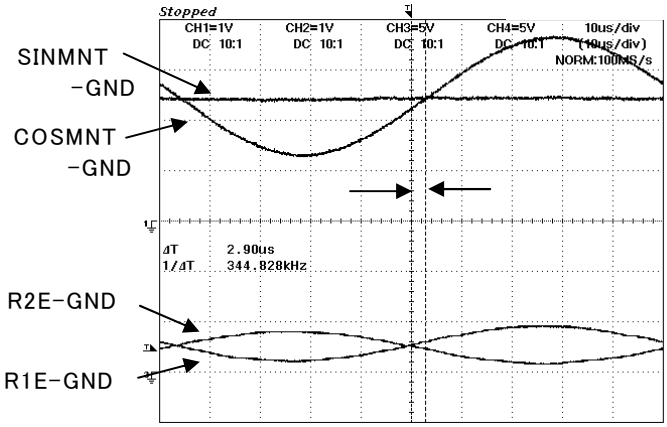


6.1.3 Check point of phase shift.

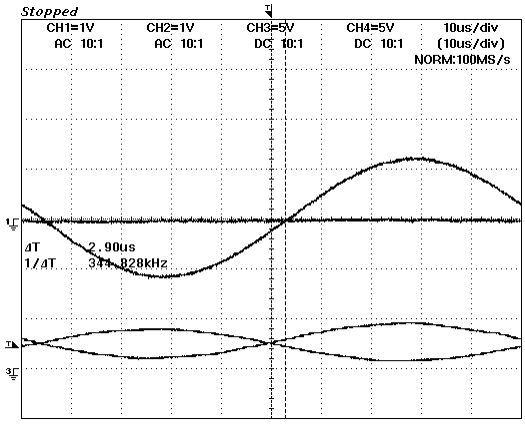
Rotating the resolver with observing a monitor signal and differential signal(R1E-R2E) of external exciting signal input, please check that phase difference between differential signal(R1E-R2E) and monitor signal(SINMNT or COSMNT) should be within ±10° . The measurement will be done at common phase position between "R1E-R2E"signal and monitor. If it exceed ±10° , please make phase adjustment at external exciting signal input circuit.

■How to convert an angle from phase shift.

Monitor out signal DC coupling example.



Monitor out signal AC coupling example.



Converted angle[deg]＝360[deg]×(time shift[μs]／exciting F period[μs]

Above example: exciting F＝10KHz → exciting F period＝100μ(＝1/10KHz)
Time shift＝2.9μs
Converted angle＝10.4deg (＝360×2.9／100)

6.2 Check Point for Digital Output

6.2.1 Check Point of Output Angle

Please check that the each digital output show your required format which you set and angle output data is changing with resolver rotation. If angle output is not change while resolver rotation or output format is different with your setting, please check a polarity of each digital input terminal. Also if output angle data does not match with actual angle or output data is not stable, refer section 6.1 and please check if there is no problem for resolver related connections.

6.2.2 Check point of abnormality Detection

“ERR” output and “ERRHLD” output should be both L-level for normal condition while ” ERRSTB” input is H-level. If this device detects some error condition, “ERR” output or “ERRHLD” output will be H-level. Then you may refer section 8.1 and please isolate the true cause of the error and remove it.

7. Function of Fault Detection

AU6802N1 has built-in test function of fault detection which detects abnormal sensor signal and abnormal R/D conversion. These error conditions output at the “ERR” or “ERRHLD” terminal. The 3 kind of contents of detection are shown below

- ・Abnormal sensor signal(breaking/down of exciting source line: R1 & R2)
- ・Abnormal sensor signal(breaking of resolver signal line: S1,S2,S3 & S4)
- ・Abnormal R/D conversion(Excessive residuals of control signal)

In this chapter, describe each detection method, typical fault detection pattern, and error reset operation.

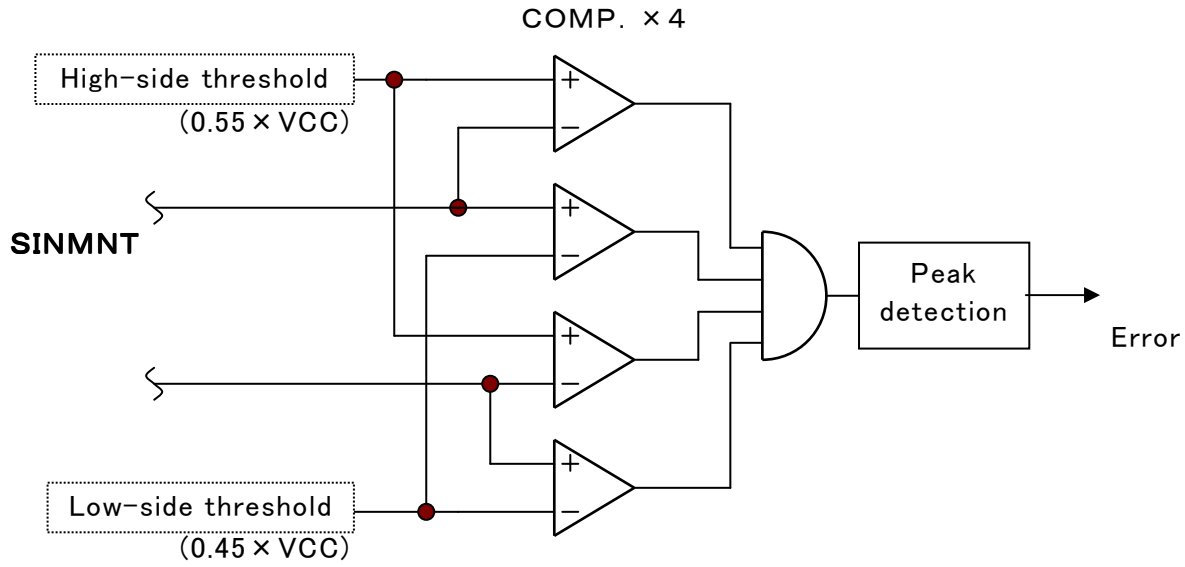
This built-in test function is independent from R/D conversion function and does not restrict the R/D conversion output by its result (i.e. any detection of abnormal state).

7.1 Abnormal sensor signal(breaking/down of exciting source lines)

7.1.1 Concept Detection

This concept is to detect smaller monitor output amplitude level then it defines as abnormal sensor signal. Breaking/down of exciting source line can not excite resolver. As a result resolver output signal will disappear and abnormal sensor signal can be detect.

7.1.2 Circuit Configuration



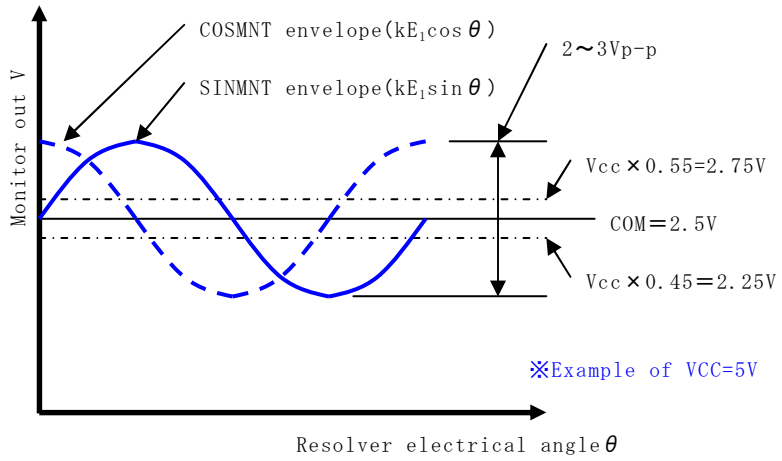
7.1.3 Detection Principle

The principle is comparison between monitor output and threshold voltage. Detect situation that the voltage magnitude of SINMNT and COSMNT are above low-side threshold and below high-side threshold. It mean both monitor amplitude is under 0.1×VCC(Vp-p)※ , and define this situation as abnormal.

※Example of VCC=5V case, detection condition is under 0.5Vp-p of both monitor amplitude.

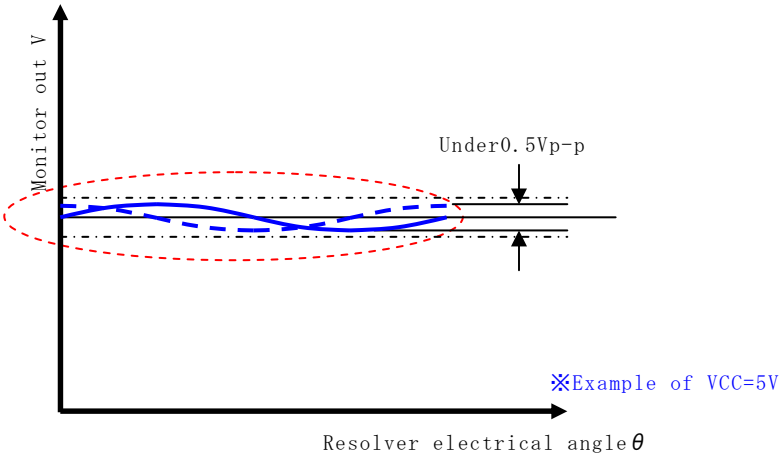
7.1.4 Relationship of threshold and **typical** abnormal detection pattern

(1)Normal



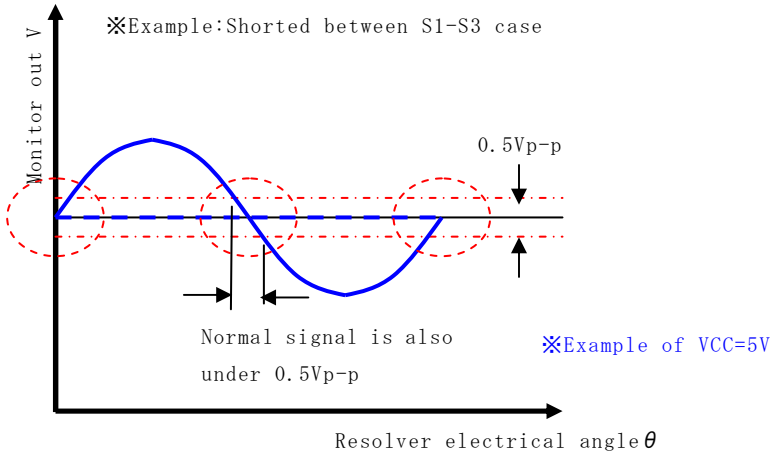
In normal monitor signal case, either SINMNT or COSMNT exceed a threshold value, then it does not detect abnormal sensor signal.

(2)Detection pattern①(Monitor amplitude is under threshold)



Breaking/down of exciting circuit or smaller monitor output will detect as abnormal signal in full angular range.

(3)Detection pattern②(Shorted between S1-S3 or S2-S4)



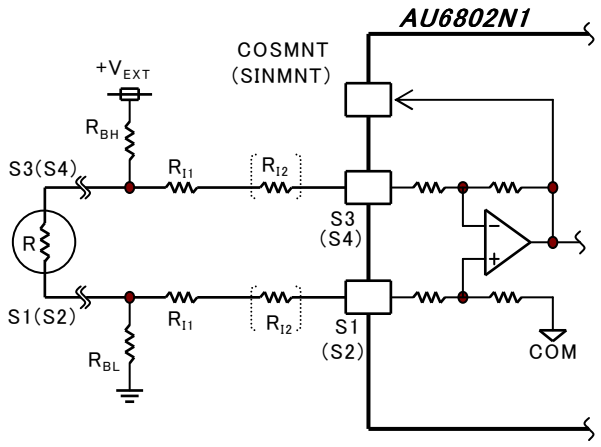
In case of short between S1-S3 or S2-S4, when normal signal amplitude go under the threshold value, error can detect in such angle range.

7.2 Abnormal sensor signal(breaking of Resolver signal lines)

7.2.1 Concept Detection

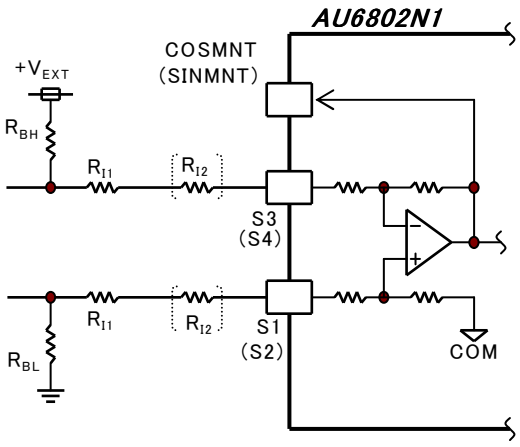
In the resolver signal input circuit, applying the external DC bias circuit will make monitor output level shifted from COM voltage of reference potential to GND side in DC. Concept detection is to detect that voltage shift.

【In view DC: Normal-resolver signal input circuit】



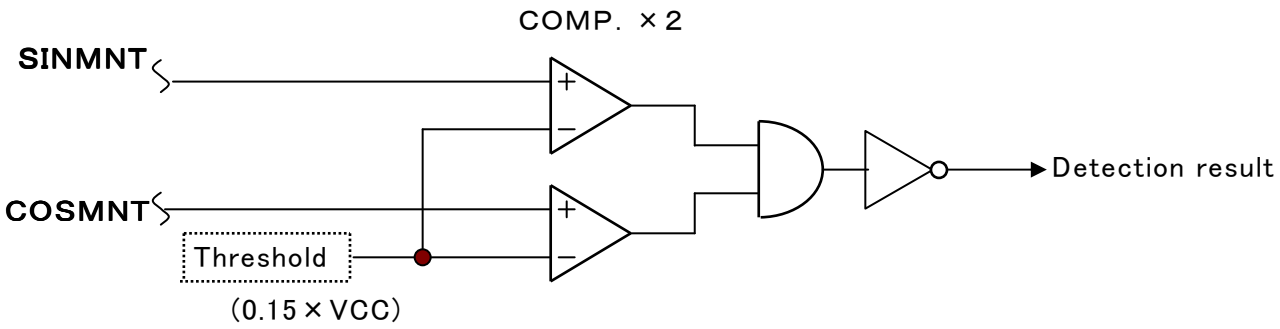
Resolver DC 【R】 ≪ DC bias 【R_{BH} or R_{BL}】, In this case Resolver terminal S1 and S3 (S2 and S4) are same DC potential. Then monitor output that is differential amplifier output is COM potential as DC reference one.

【In view DC: Breaking-resolver signal input circuit】



During breaking line, " +VEXT-GND " entered to differential amplifier circuit input. Then monitor output shift to GND side against COM potential as reference.

7.2.2 Circuit Configuration



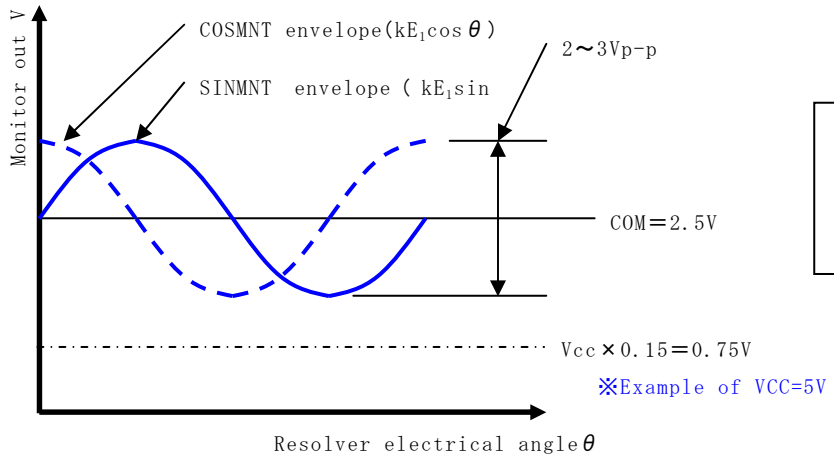
7.2.3 Detection Principle

The principle is comparison between monitor output and threshold voltage. If voltage magnitude of SINMNT or COSMNT exceed down the threshold value(0.15 X VCC※), it is detected as fault situation.

※Example of VCC=5V case, detection condition is under $0.75V_{DC}$ of monitor output voltage.

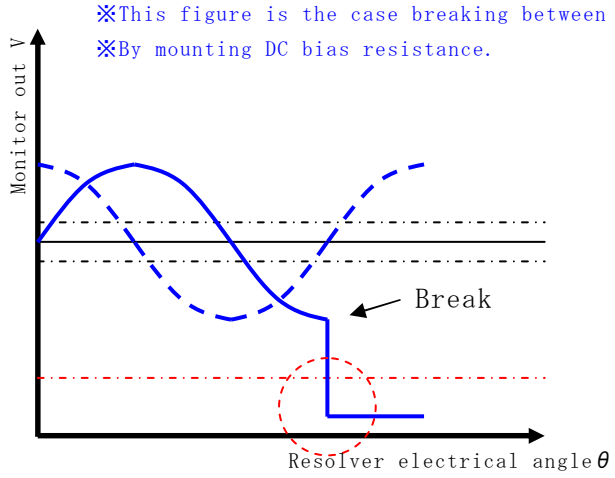
7.2.4 Relationship of threshold and Typical abnormal detection pattern

(1)Normal



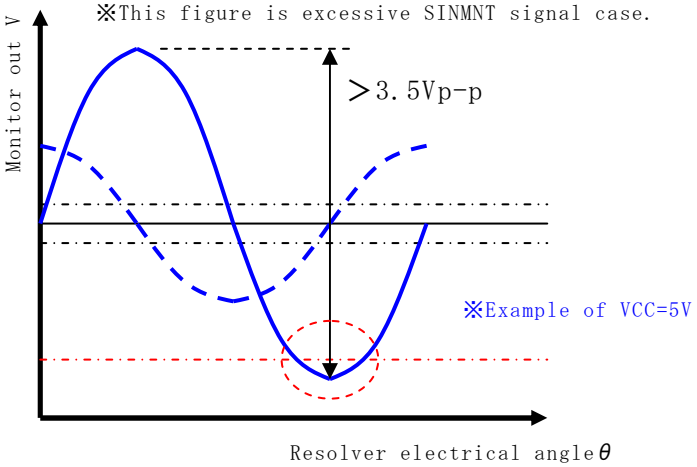
In normal monitor signal case, both SINMNT and COSMNT exceed a threshold value, then it does not detect abnormal sensor signal.

(2)Detection pattern③(Breaking between S1-S3 or S2-S4)



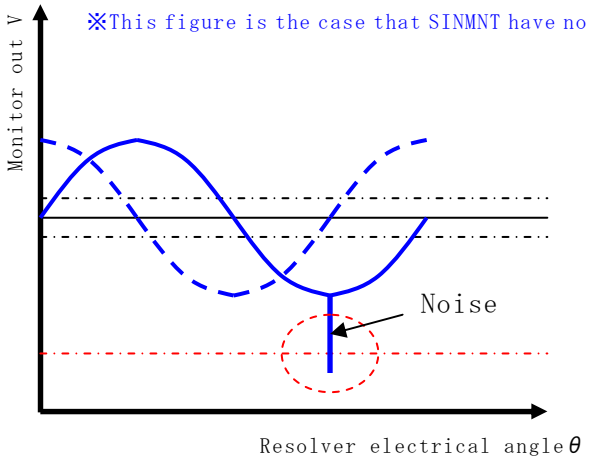
In case of breaking signal line, monitor output will be less than threshold DC level and it is detected as fault.

(3)Detection pattern④(Excessive monitor output)



In case of SINMNT or COSMNT is excessive and cross the threshold, it is detected as fault.

(4)Detection pattern⑤(Noise superimposed)



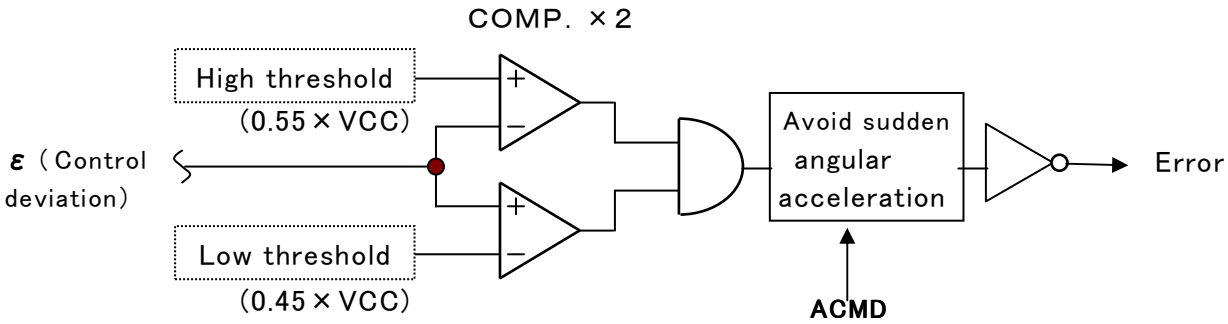
Due to a noise, monitor output cross the threshold down. Then it is detected as fault.

7.3 Abnormal R/D conversion(Excessive control deviation)

7.3.1 Concept Detection

This product adopted digital tracking method (Refer section 1.3 or 9.1) as R/D conversion system, and this method is one of the negative feedback control of closed-loop configuration. In such a system, normally control deviation (ε) should be "0". This concept detection is that the excessive control deviation means out of control and this situation is detected as abnormal.

7.3.2 Circuit Configuration



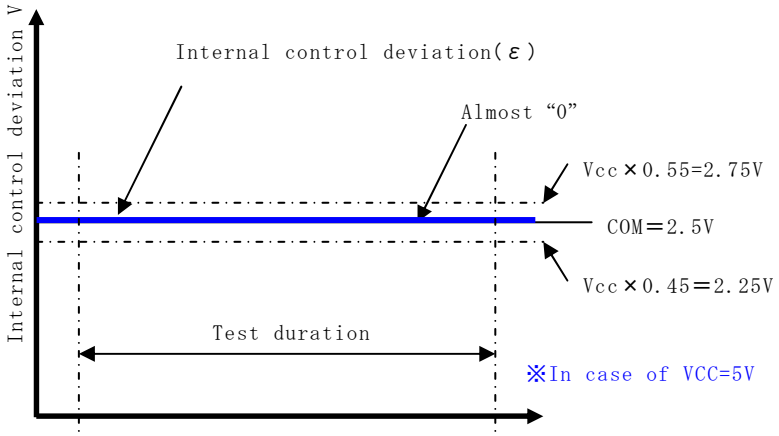
7.3.3 Detection Principle

This detection principle is to compare the internal control deviation(*1) and the threshold value. If there are situation that the absolute value of internal control deviation is less than low threshold or bigger than high threshold(*2), and if this situation is over 50% of test duration(*3), then it is detected as fault.

※1 A internal control deviation signal can not be verified by this product's terminals.
※2 In case of VCC=5V, anomaly detection condition is excess threshold(less than 2.25 V_{DC}, bigger than 2.75 V_{DC})of internal control voltage.
※3 "ACMD=H" condition is 5ms、"ACMD=L" condition is 120ms.

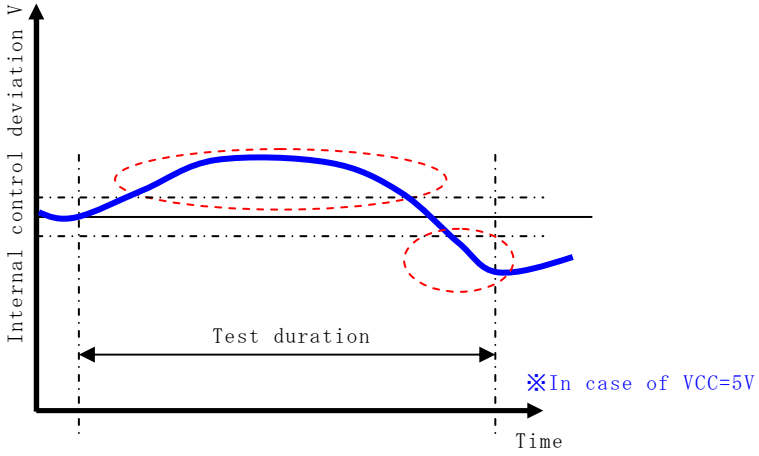
7.3.4 Relationship of threshold and Typical abnormal detection pattern

(1) Normal



In the state that have been successfully R/D converted, control deviation is almost "0". Then it is not detected as fault.

(2) Detection pattern⑥(Excessive control deviation)

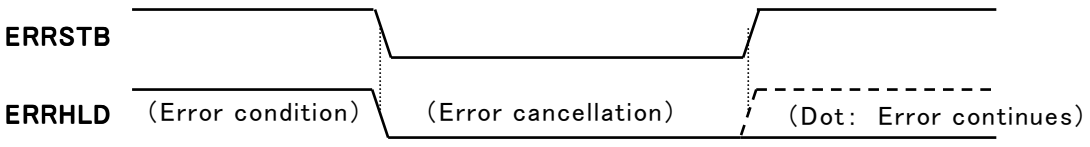


There is an abnormal R/D conversion situation (control deviation exceed the threshold), and if such situation is over 50% of test duration, it is detected as fault.

7.4 Error reset

ERRHLD output is generated when an error occurred, and it can be cleared by setting ERRSTB=Low.

■Error reset operation waveform



※ Refer 9.8 for detail timing.

※ Please use ERRHLD output after it is surely cleared by ERRSTB signal. If the error is not released even after error reset, please eliminate the true error factor according to the section 8.1.

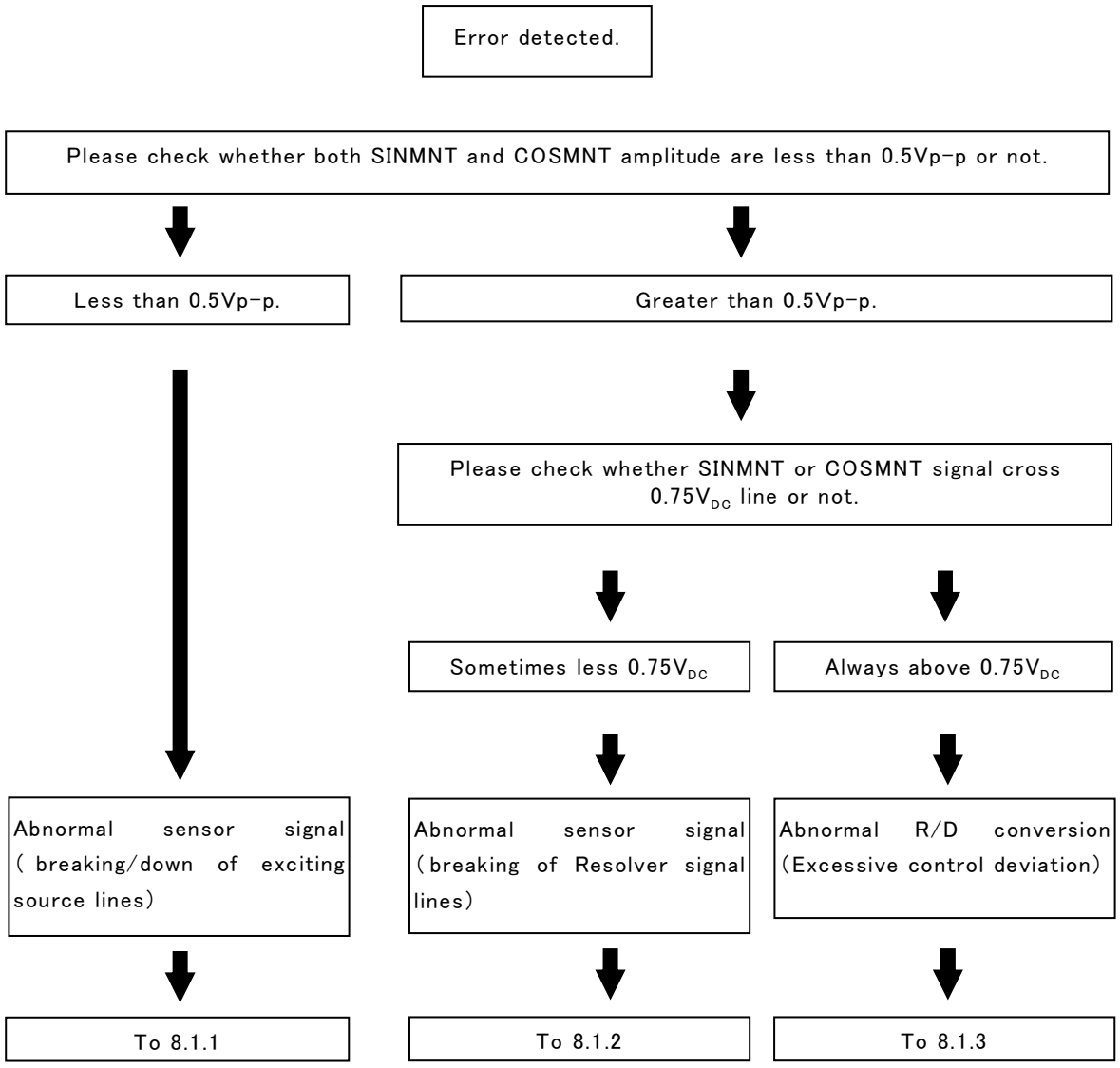
8. If you think troubleshooting

In this chapter, there are corresponding examples for the case of error detected by the function of fault detection, and for the case of strange angle output data. Please check these examples for your troubleshooting and operation check.

8.1 In case of error detection

When an error is detected (ERR or ERRHLD output are "H" level), refer to the following troubleshooting flow. Firstly please perform to estimate reason of fault detection, and error factor should be identified and eliminated according to the procedure of chapter 8.1.1 or later. Regarding the operation of fault detection function, please refer chapter 7.

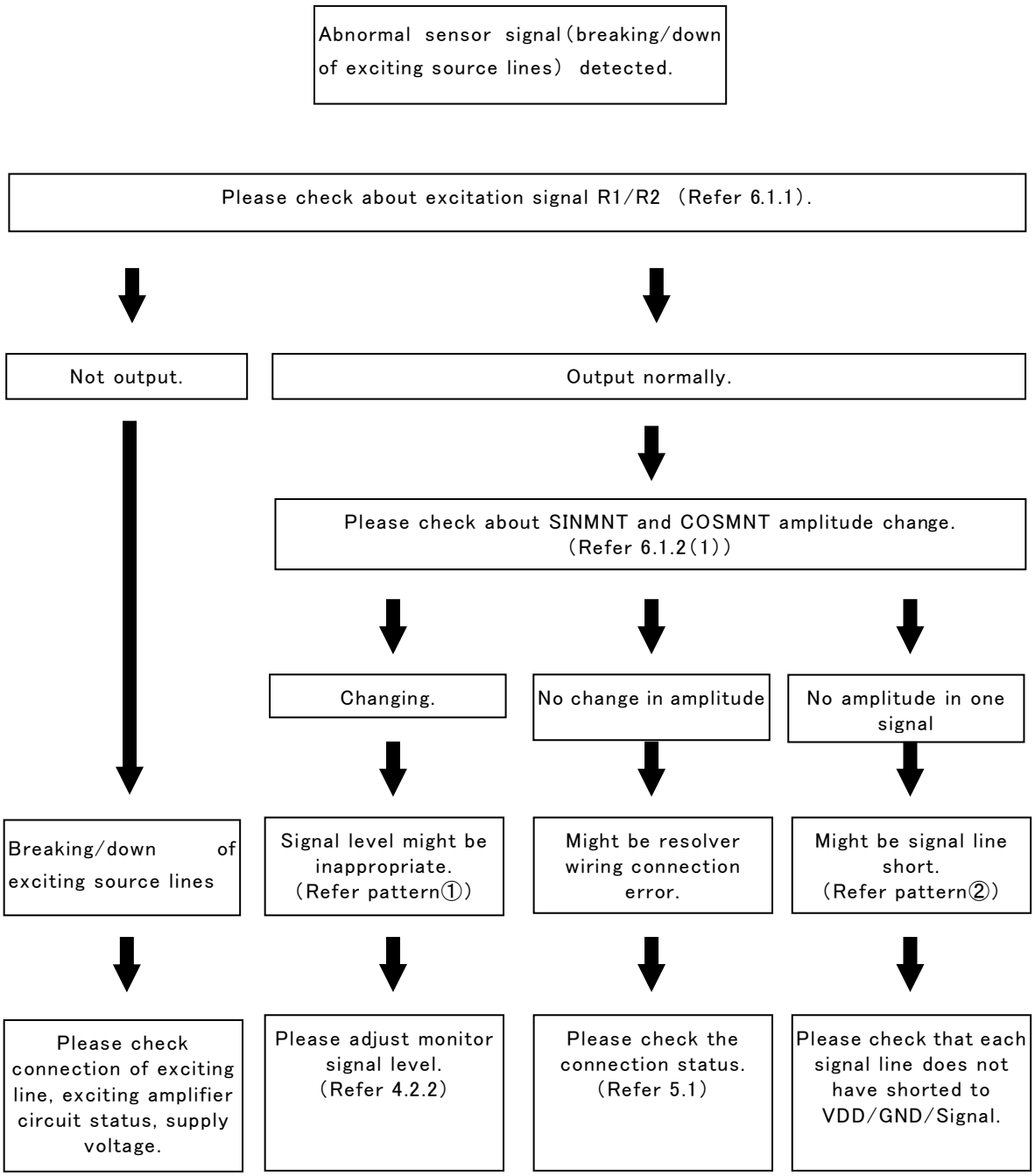
■Troubleshooting flow of error



8.1.1 Suspicion of Abnormal sensor signal(breaking/down of exciting source lines)

In case of suspicion the breaking/down of exciting source lines, true error factor should be identified and eliminated according to the below troubleshooting flow.

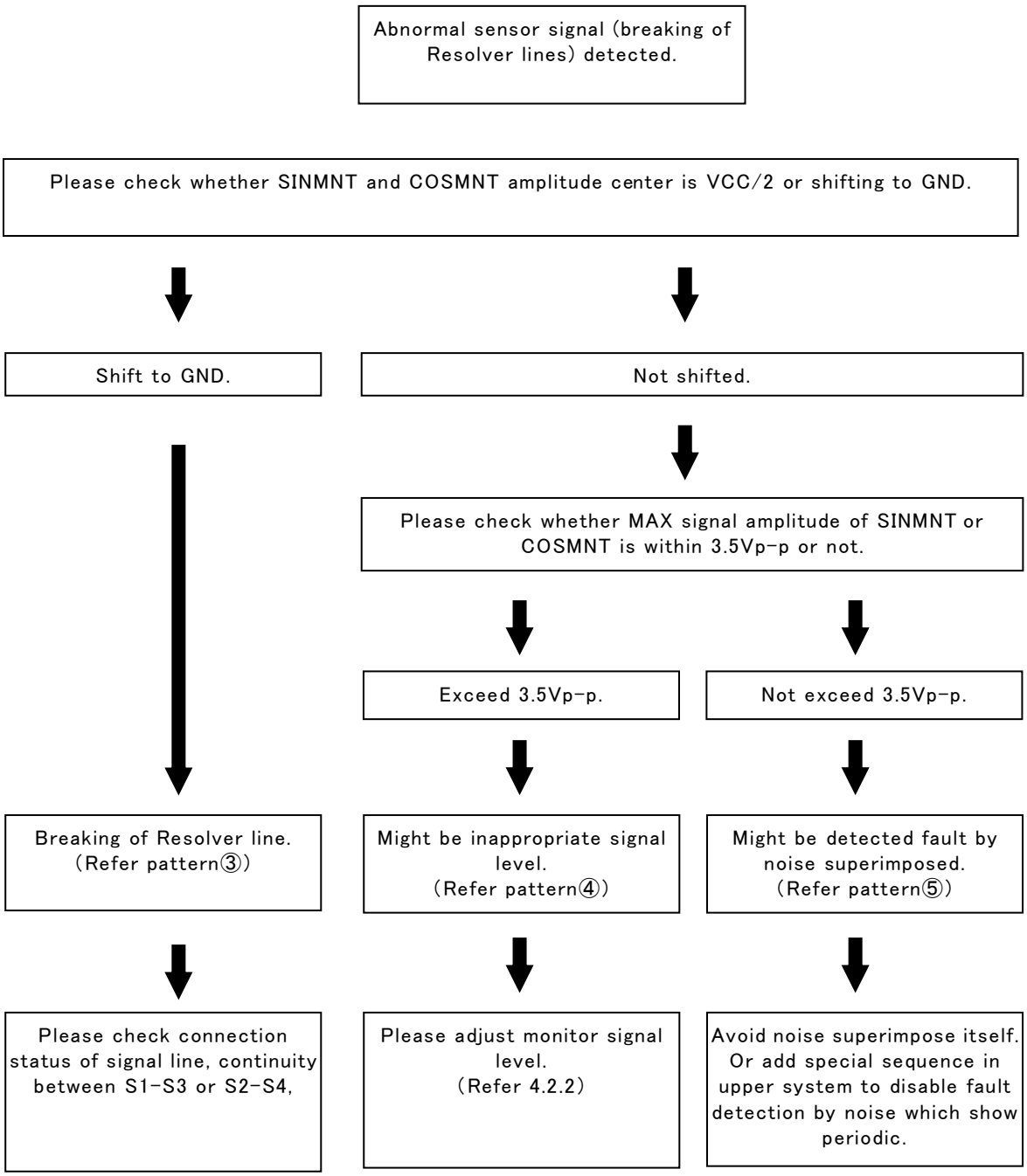
■Troubleshooting flow of detecting break/down of exciting source lines



8.1.2 Suspicion of Abnormal sensor signal(breaking of Resolver signal lines)

In case of suspicion the breaking of resolver signal lines, true error factor should be identified and eliminated according to the below troubleshooting flow.

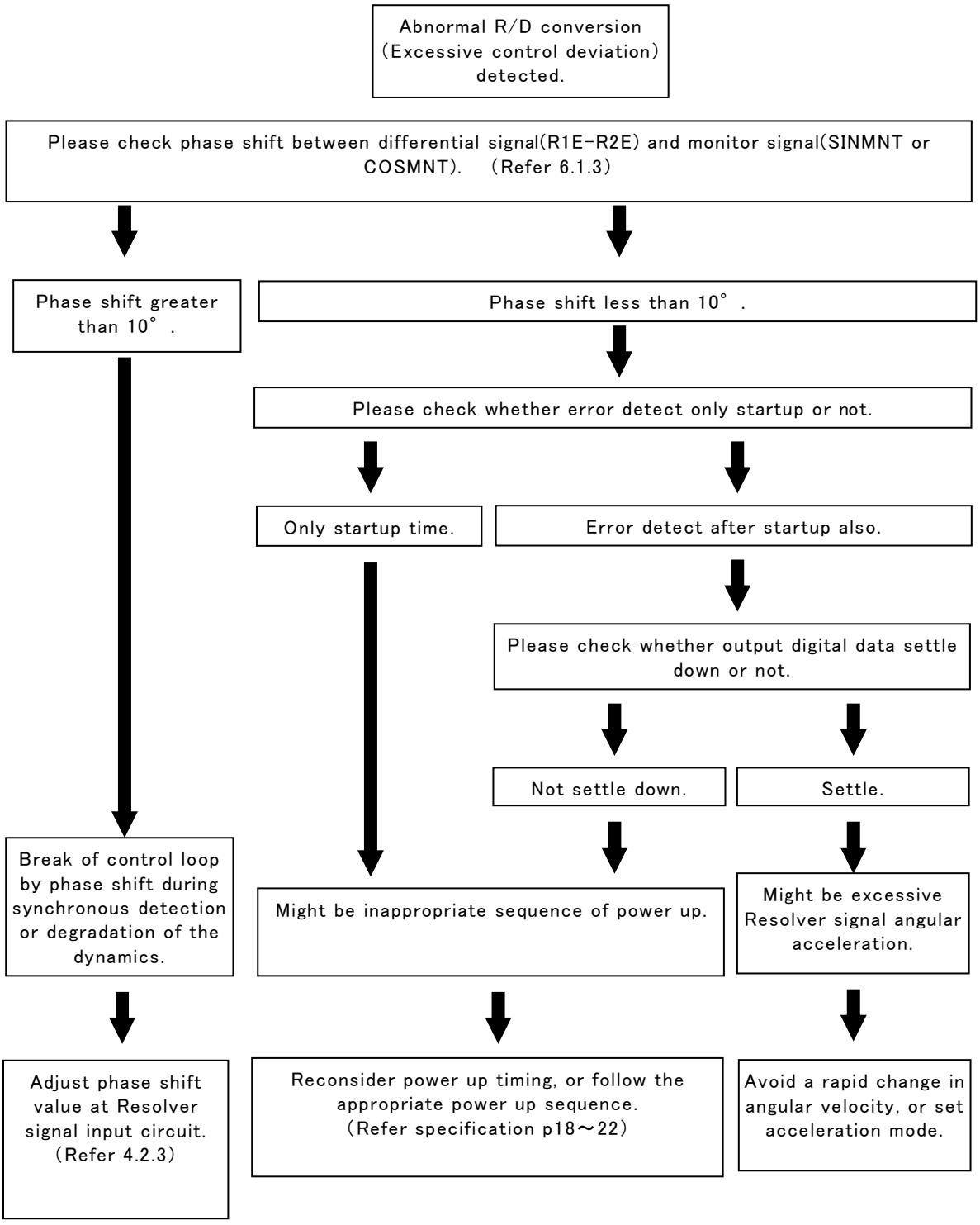
■Troubleshooting flow of detecting break of Resolver signal lines



8.1.3 Suspicion of Abnormal R/D conversion(Excessive control deviation)

In case of suspicion the abnormal R/D conversion, true error factor should be identified and eliminated according to the below troubleshooting flow.

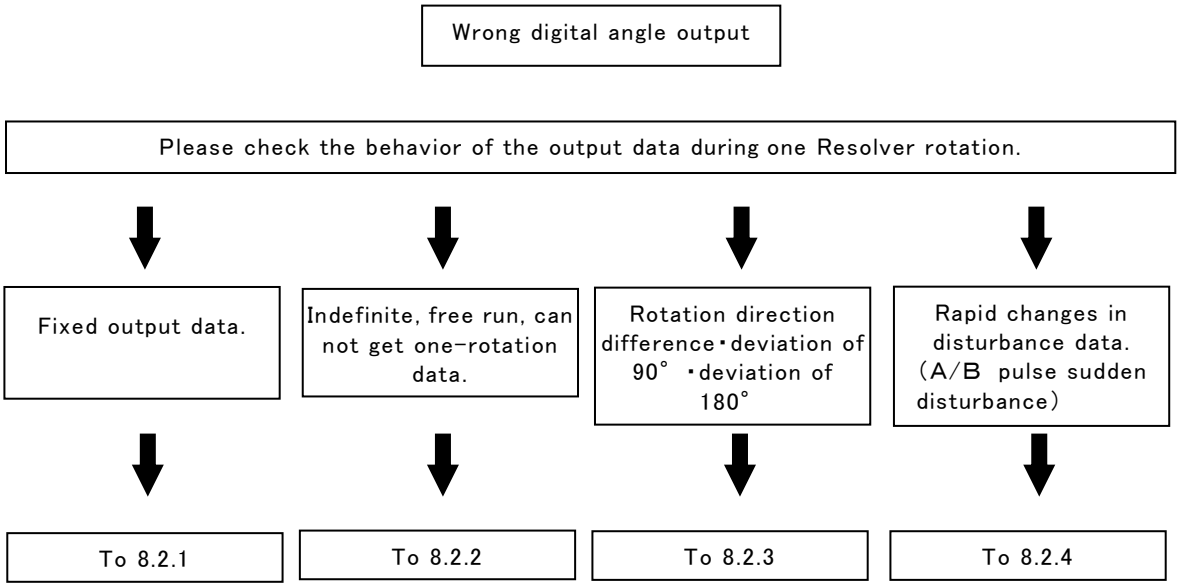
■Troubleshooting flow for Abnormal R/D conversion detection.



8.2 In case of wrong angle data

Despite the rotating Resolver, angle output data is not changed, or output shows the different format data, or output data is not fit to actual angle. In such case, please follow below troubleshooting flow and identify the behavior of the output data. Then please improve this error condition by the procedure described in chapter 8.2.1 and later.

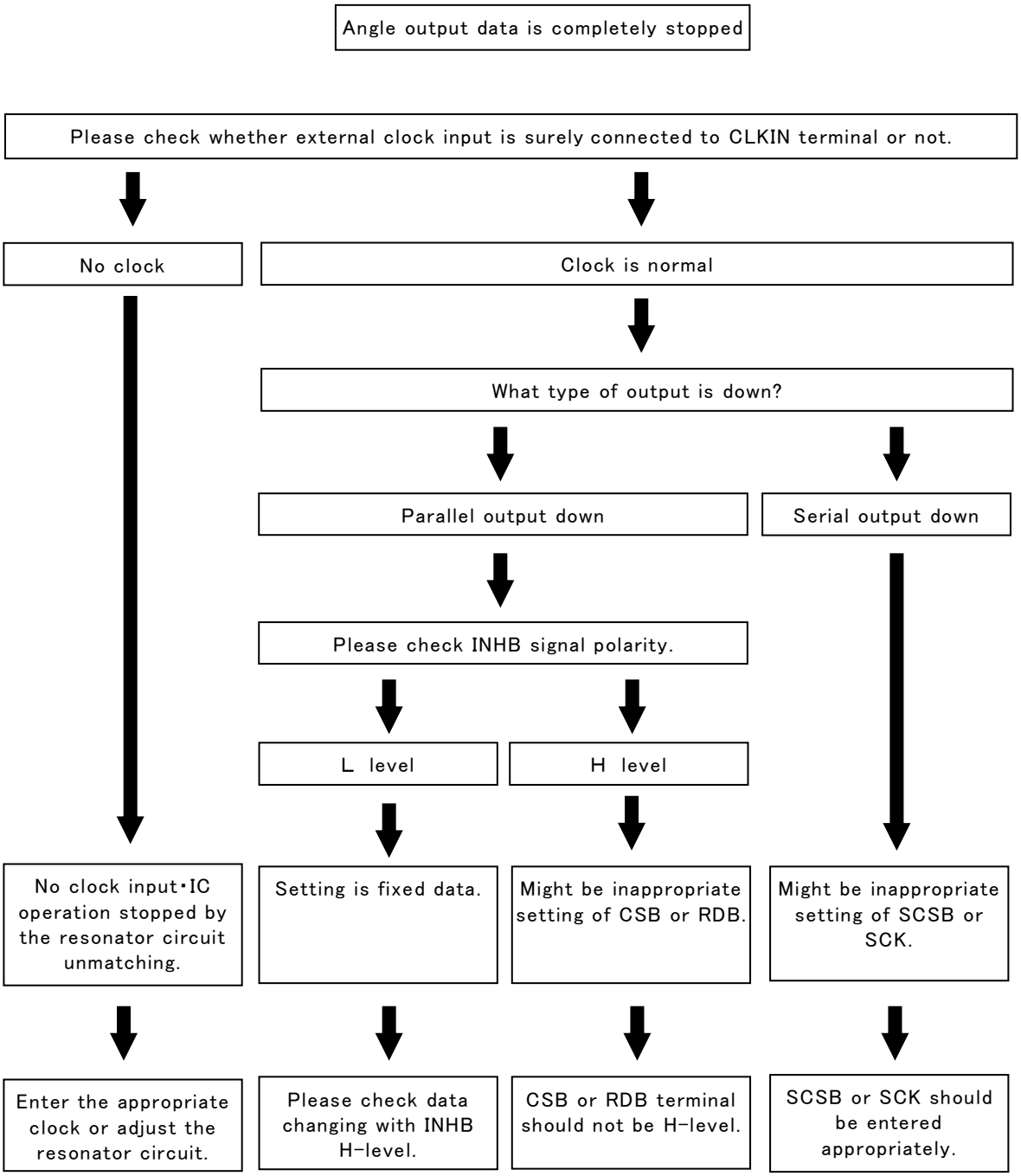
■Troubleshooting flow of wrong digital angle data.



8.2.1 In case of angle data output is stopped

In case of angle output data is completely stopped, please follow below troubleshooting flow and identify the factors, and then improve your system.

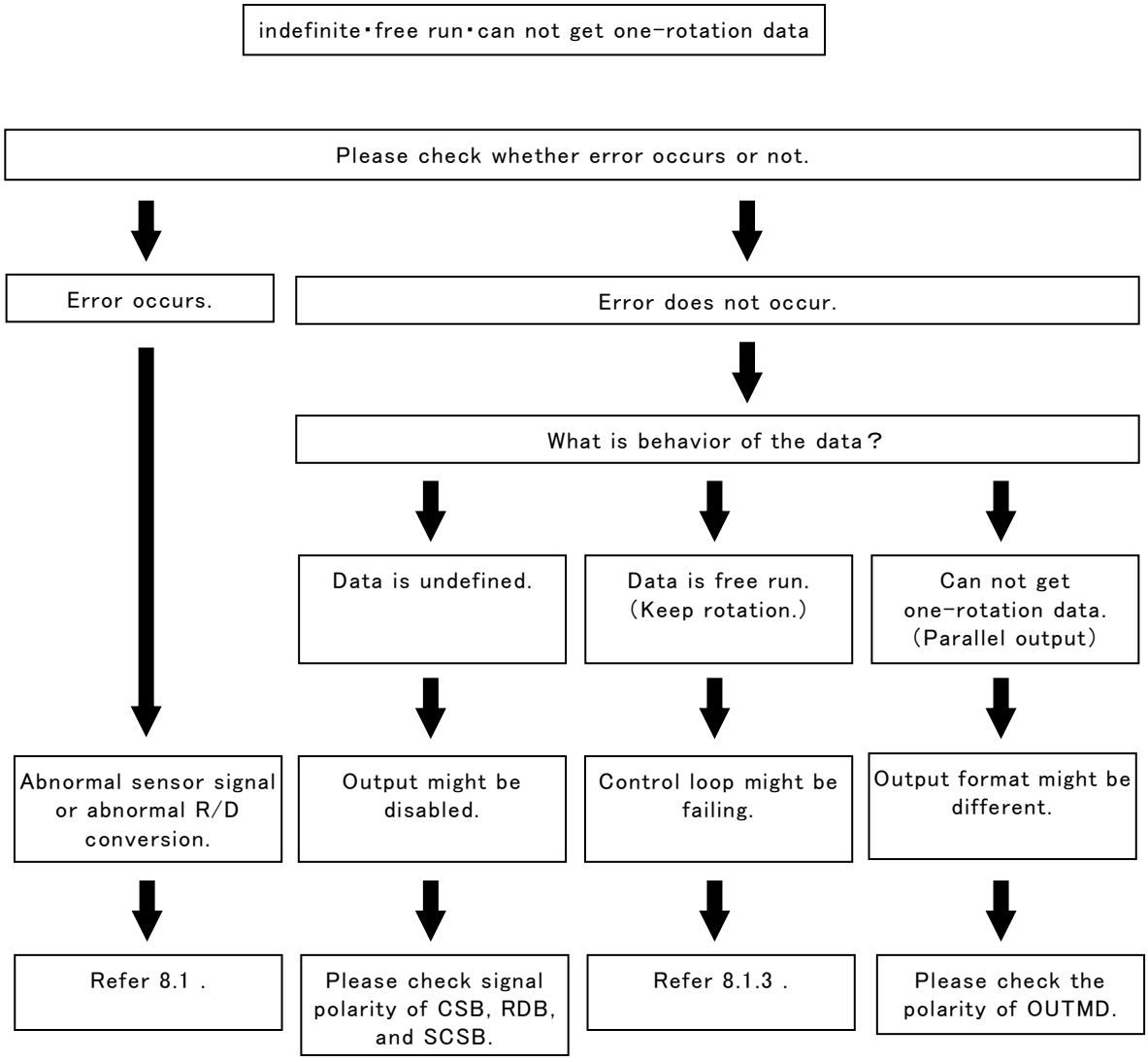
■Troubleshooting flow of fixed output.



8.2.2 In case of indefinite, free run, can not get one-rotation data

In case of angle output data is indefinite, free run, might not get one-rotation data, please follow below troubleshooting flow and identify the factors, and then improve your system.

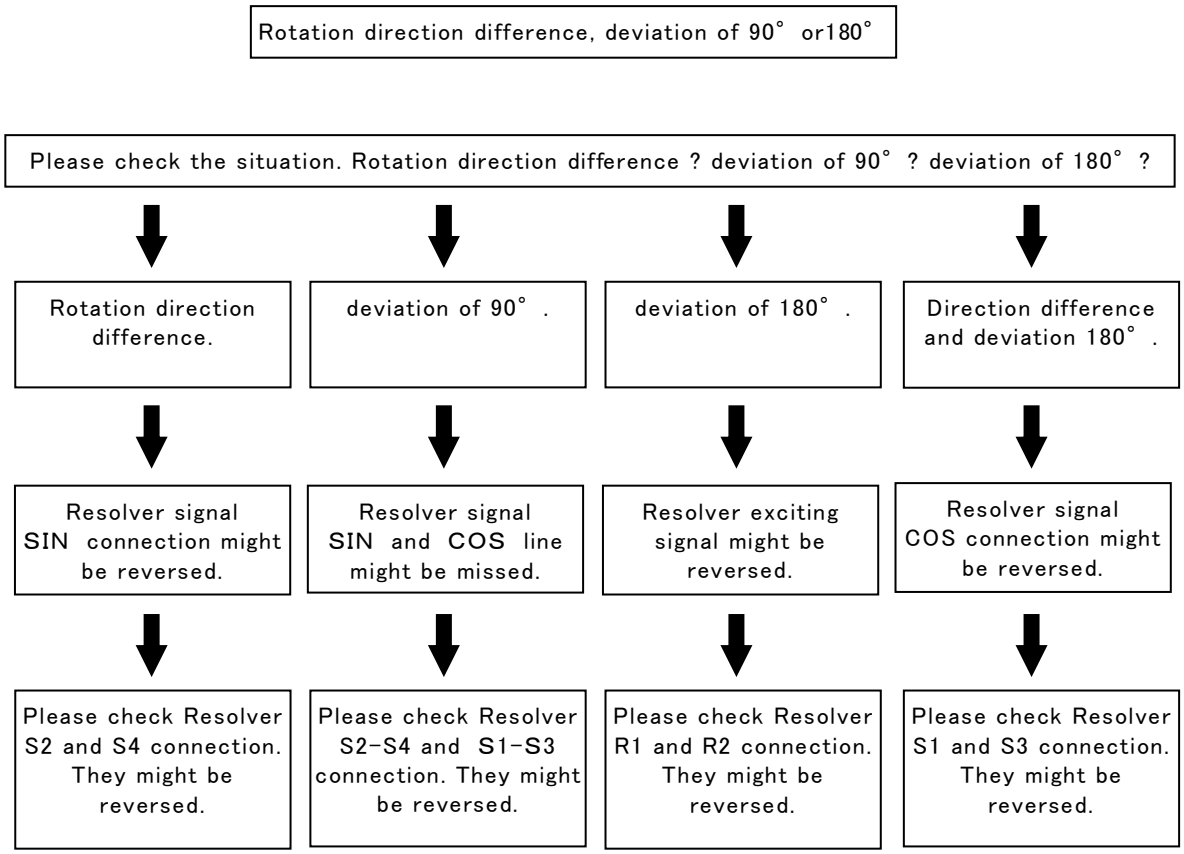
■Troubleshooting flow of indefinite, free run, can not get one-rotation data.



8.2.3 In case of rotation direction difference, deviation of 90° or 180°

In case of angular output data shows different rotation direction or there might be angular displacement of 90° or 180° , please follow below troubleshooting flow and identify the factors, and then improve your system.

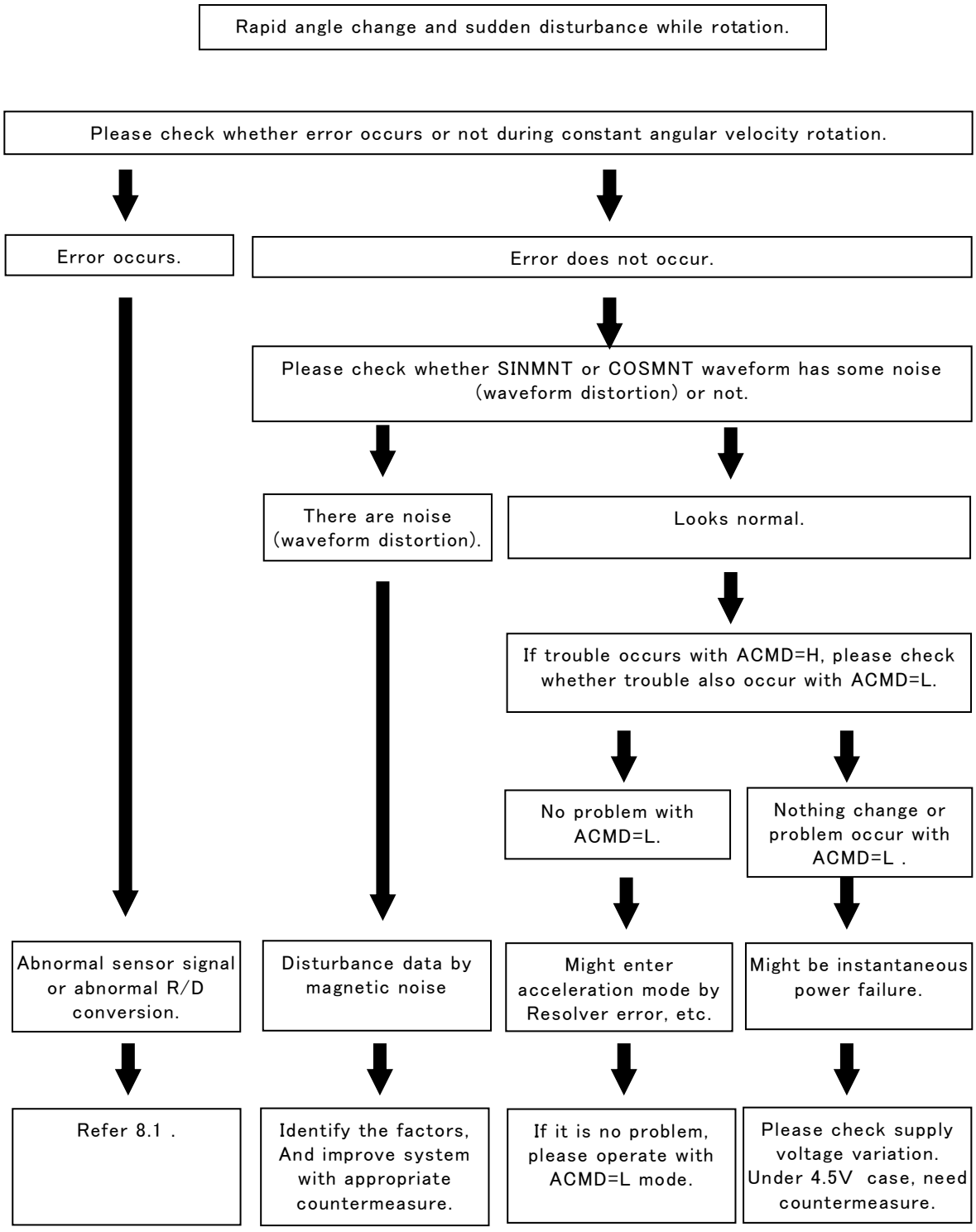
■Troubleshooting flow of rotation direction difference, deviation of 90° or 180° .



8.2.4 In case of rapid change in the output angle data and disturbance

In case of rapid change in the output angle data or a sudden disturbance while rotation, please follow below troubleshooting flow and identify the factors, and then improve your system.

■Troubleshooting flow of rapid change in the output angle data and disturbance



8.3 If the situation does not improve

If the situation does not improve even if section 8.1 or 8.2 steps perform, and if there is another phenomenon which does not mention in this manual, please contact us with waveforms when an error occur (appropriate abnormal signal, SINMNT, COSMNT) and also inform us about detail troubled circuit information.

9. Electrical characteristics

9.1 Absolute maximum rating

Items	Symbol	Absolute maximum rating	Unit
Power supply voltage	VCC	−0.3～+7.0	V
	VDD	−0.3～+7.0	V
Analog input voltage	V_{Ia}	−0.3～+7.0	V
Digital input voltage	V_I	−0.3～VDD+0.3	V
Digital output current	I_O	−10～+10	mA
Operating temperature	T_{opr}	−40～+125	℃
Storage temperature	T_{stg}	−65～+150	℃
Allowable loss	P_D	245	mW

※ If you use the IC beyond the absolute maximum rating, it may cause permanent damage to the IC.

9.2 Power-related characteristic

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Power supply voltage	VCC	4.75	5.0	5.25	V	Recommended power supply voltage. VCC, VDD must be used at the same potential.
	VDD	4.75	5.0	5.25	V	
Reset release voltage	Vrsth	3.9	−	4.4	V	Power-On-Reset release voltage
Reset voltage	Vrstl	3.7	−	4.2	V	Power-On-reset voltage
Reset voltage hysteresis	Vrhys	−	0.2	−	V	Vrsth-Vrstl
Supply current	I_{CC}	−	30	45	mA	Current consumption without load.

9.3 R/D conversion characteristic

■ 10 Bits resolution setting

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Resolution			10		Bit	A number of divisions per electrical angle.
Conversion accuracy		−2	0	+2	LSB	Absolute error of the electrical angle input in a stationary state.
Settling time 1			1		ms	ACMD="H" Input step of 180° electrical angle Settling range : ±8LSB max.
Settling time 2			15		ms	ACMD="L" Input step of 180° electrical angle Settling range : ±8LSB max.
Maximum angular velocity		240,000			min^{-1}	Capable of following angular velocity range (electrical angle)
Maximum angular acceleration		256,000			rad/s^2	Capable of following angular acceleration range (electrical angle)
Responsibility		−0.2		+0.2	deg./ $10{,}000min^{-1}$	Output response delay in a constant angle velocity. (Equivalent to 3.33 μ s)

■ 12 Bits resolution setting

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Resolution			12		Bit	A number of divisions per electrical angle.
Conversion accuracy		−4	0	+4	LSB	Absolute error of the electrical angle input in a stationary state.
Settling time 1			2.5		ms	ACMD="H" Input step of 180° electrical angle Settling range : ±8LSB max.
Settling time 2			60		ms	ACMD="L" Input step of 180° electrical angle Settling range : ±8LSB max.
Maximum angular velocity		60,000			min^{-1}	Capable of following angular velocity range (electrical angle)
Maximum angular acceleration		64,000			rad/s^2	Capable of following angular acceleration range (electrical angle)
Responsibility		−0.4		+0.4	deg./ $10{,}000min^{-1}$	Output response delay in a constant angle velocity. (Equivalent to 6.67 μ s)

9.4 Failure detection characteristic

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Abnormal sensor signal(breaking/down of exciting source lines)						
Detection threshold High-side		0.523 ×VCC	0.55 ×VCC	0.577 ×VCC	V	VCC=VDD=5.0V Compared to the monitor output voltage (Min., Max. are reference)
Detection threshold Low-side		0.428 ×VCC	0.45 ×VCC	0.472 ×VCC	V	VCC=VDD=5.0V Compared to the monitor output voltage (Min., Max. are reference)
Detection time		–	–	0.2	ms	Time required detecting fault.
Abnormal sensor signal(breaking of Resolver signal lines)						
Detection threshold		0.143 ×VCC	0.15 ×VCC	0.157 ×VCC	V	VCC=VDD=5.0V Compared to the monitor output voltage (Min., Max. are reference)
Detection time		–	–	0.1	ms	Time required detecting fault.
Abnormal R/D conversion(Excessive control deviation)						
Detection threshold High-side		0.523 ×VCC	0.55 ×VCC	0.577 ×VCC	V	VCC=VDD=5.0V Compare to the absolute value of internal control deviation (Min., Max. are reference)
Detection threshold Low-side		0.428 ×VCC	0.45 ×VCC	0.472 ×VCC	V	VCC=VDD=5.0V Compare to the absolute value of internal control deviation (Min., Max. are reference)
Required time period for judgment		–	5	–	ms	Acceleration mode "ON" It is judged as an internal error when the probability of excessive control residuals 50% in the average value for the period.
		–	120	–	ms	Acceleration mode "OFF" It is judged as an internal error when the probability of excessive control residuals 50% in the average value for the period.

※ In case of the continuous time of failure is shorter than above detection time, there is possibility not to detect failure.

9.5 Analog signal characteristic

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
Signal source output for exciting Resolver(RSO)						
Output voltage	V_{RSO}	1.8	2.0	2.2	Vp-p	VCC=VDD=5.0V、COM=2.5V Balanced potential to COM
Output frequency 1			F_{CLK}/ 1000		Hz	Frequency selection setting FSEL1="L"、FSEL2= "H" (F_{CLK}=External CLK-IN Frequency)
Output frequency 2			F_{CLK}/ 2000		Hz	Frequency selection setting FSEL1="H"、FSEL2= "H" (F_{CLK}= External CLK-IN Frequency)
Load impedance		1.0			kΩ	
Common output(COM)						
Output voltage	V_{COM}	0.5 × VCC -5%	0.5 × VCC	0.5 × VCC +5%	V	
Load impedance		1.0			kΩ	
External signal input for exciting Resolver(R1E, R2E)						
Input resistance		13	20	35	kΩ	
Input resistance ratio		0.99	1.00	1.01		Resistance variation±1%
Input frequency		8	-	20.4	kHz	
Input voltage range		0	-	5	V	COM=2.5V
Resolver signal input(S1～S4)						
Input resistance		13	20	27	kΩ	
Input resistance ratio		0.99	1.00	1.01		Resistance variation±1%
Input gain		3.47	3.5	3.53		Internal feedback R/Internal input R
Input frequency		8	-	20.4	kHz	
Input voltage		-	-	1.1	Vp-p	Differential input
Resolver signal monitor output(SINMNT, COSMNT)						
Max. Output voltage range		3.5	-	-	Vp-p	
Load impedance		10	-	-	kΩ	Allowable load impedance of SINMNT, COSMNT

9.6 DC characteristic of digital signal

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
High level input voltage	V_{IH}	2.0	–	VDD	V	Recommended input "H" voltage for all digital input terminals.
Low level input voltage	V_{IL}	0	–	0.8	V	Recommended input "L" voltage for all digital input terminals.
Input hysteresis voltage	V_H	–	0.2	–	V	
Input pull-up resistance	R_{PU}	30	50	100	kΩ	Pull-up resistor value of digital input terminal.
Input leakage current	I_L	–	–	-250	μA	V_I=DGND
High level output voltage	V_{OH}	VDD-0.1	–	–	V	I_{OH}=0mA
		VDD-0.4	–	–	V	I_{OH}=-8mA
Low level output voltage	V_{OL}	–	–	0.1	V	I_{OL}=0mA
		–	–	0.4	V	I_{OL}=8mA

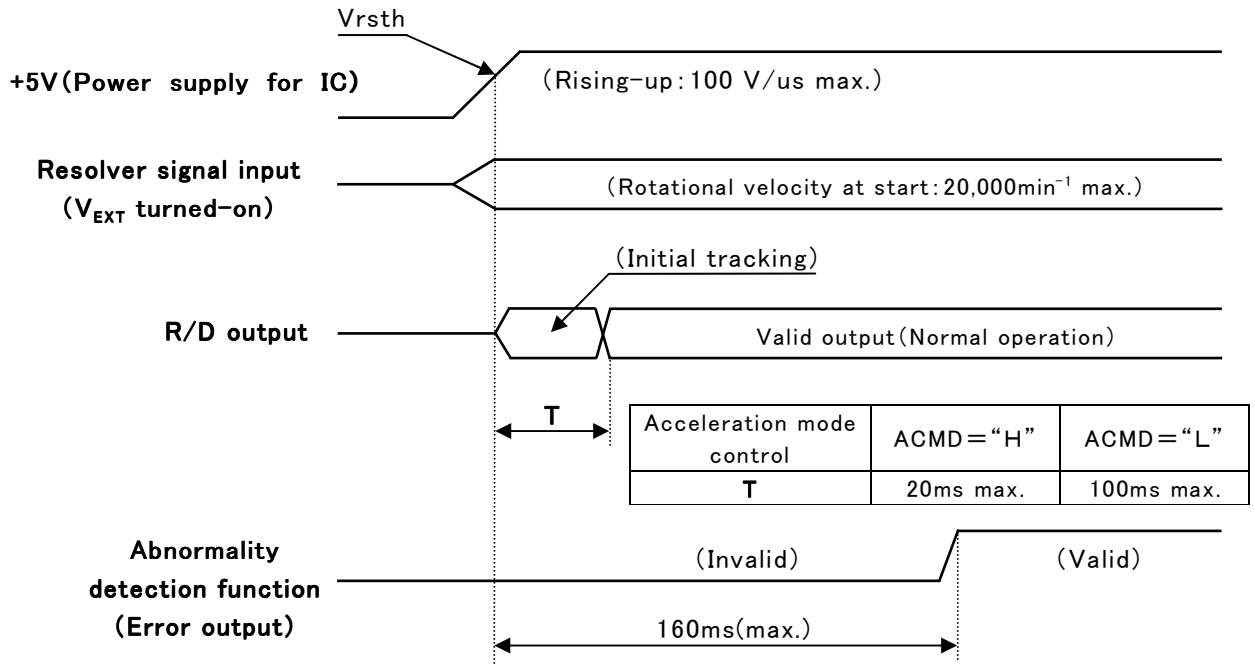
9.7 AC characteristics of digital signal

Items	Symbol	Min.	Typ.	Max.	Unit	Remarks and conditions
External CLK input frequency	F_{CLK}	18	20	20.4	MHz	
Serial CLK input frequency	F_{SCK}	–	–	2	MHz	
Input rising-up time	tri	0	–	1.0	ms	
Input falling-down time	tfi	0	–	1.0	ms	
Output rising-up time	tr	–	1.2	2.2	ns	C_L=15pF
Output falling-down time	tf	–	1.2	2.2	ns	C_L=15pF
Propagation delay time (Input buffer)	tpd	–	–	7.6	ns	
Propagation delay time (Output buffer)	tpd	–	–	8.9	ns	C_L=15pF

(Note) Rising-up/falling-down time of output means the time required to pass through the voltage between 0.3V and 2.7V.

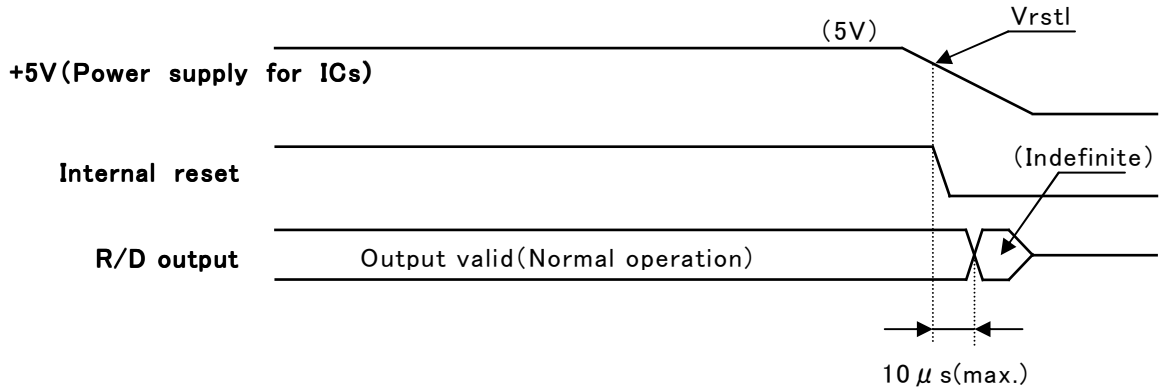
9.8 Timing diagram

■ Timing of power ON

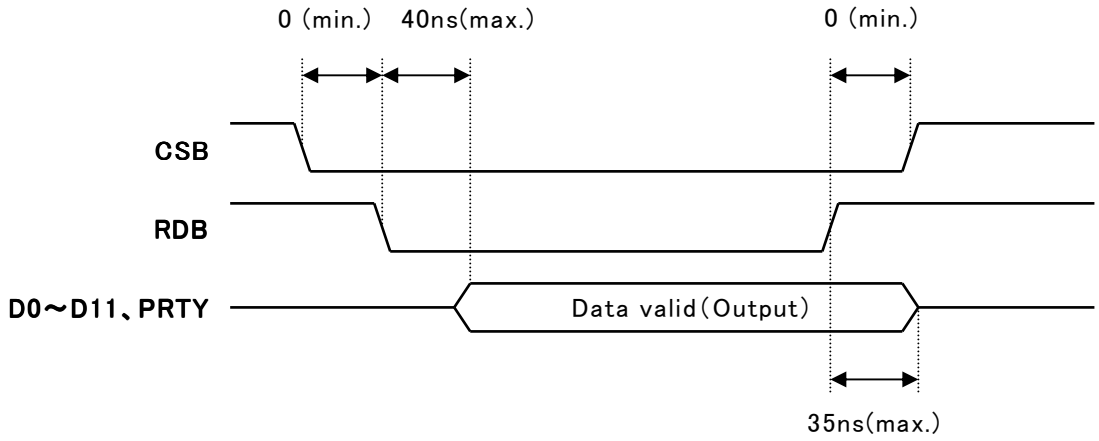


※ This shows the boot sequence recommended. . +5V(Power supply for ICs:VCC、VDD) and the power supply for exciting amplifier of Resolver(V_{EXT}) should be turned on at the same time. Or +5V should be turned on later.
Otherwise please refer the specification p18～22.

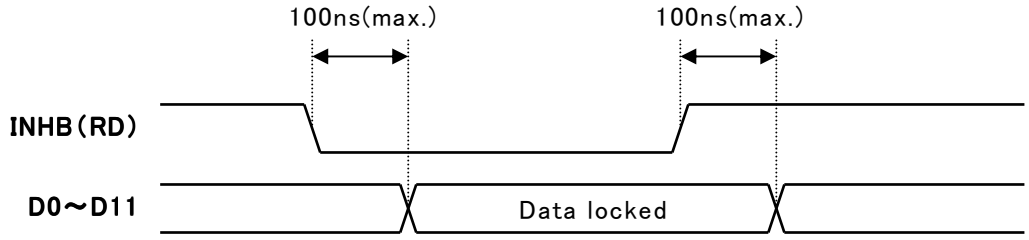
■ Timing of power OFF



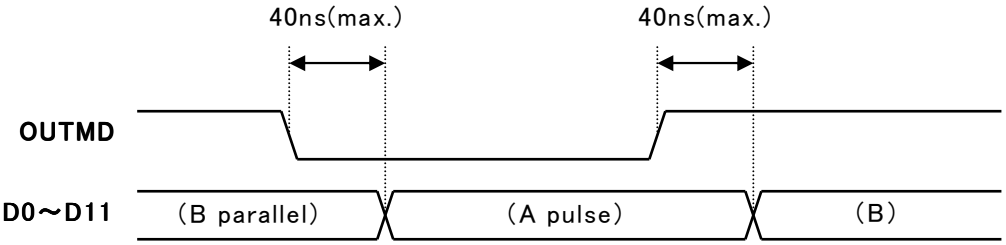
■ Timing of bus control



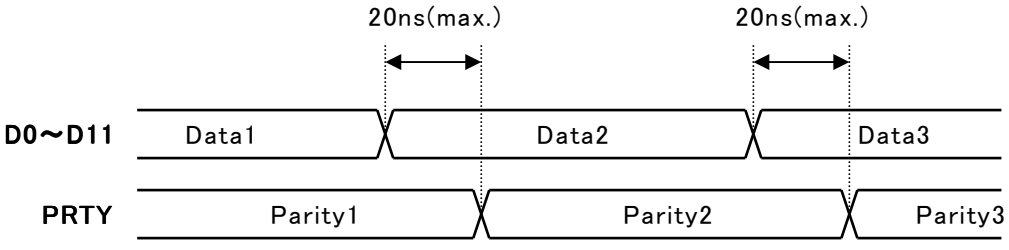
■ Timing of INHB(RD) signal



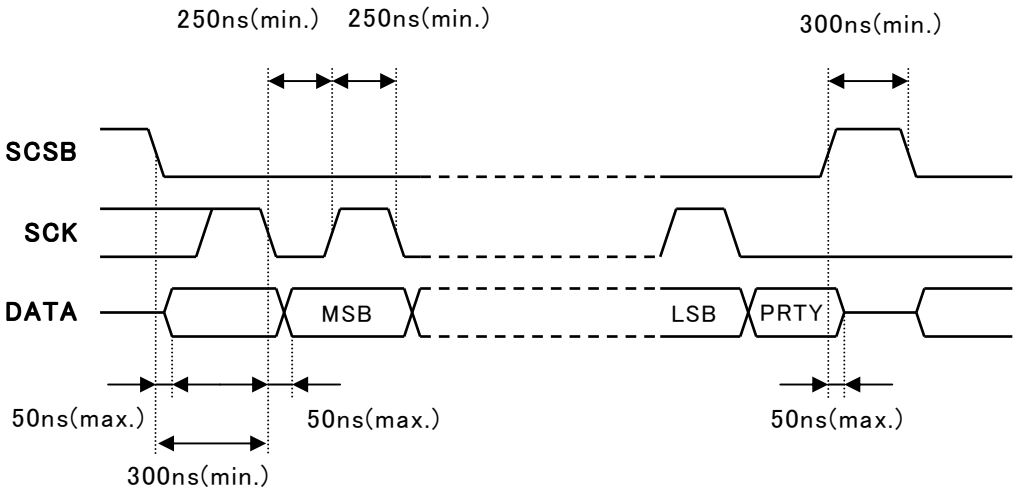
■ Timing of OUTMD signal



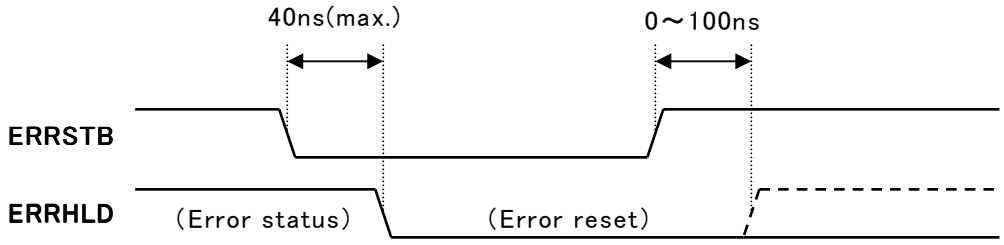
■ Timing of PRTY signal



■ Serial output operation **waveform**



■ Timing of error reset



10. Appendix

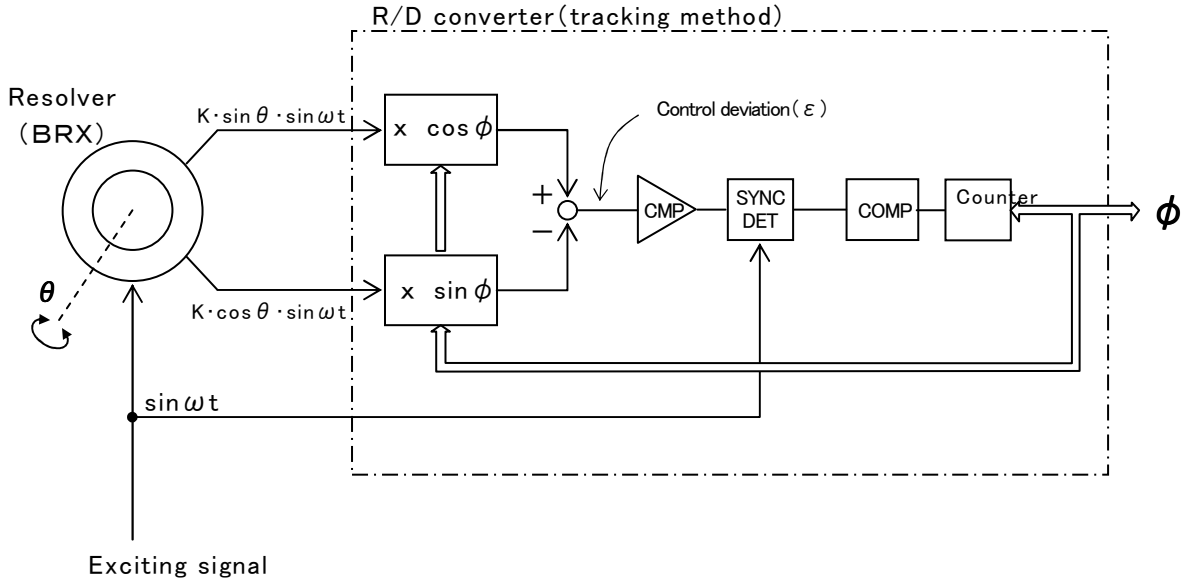
10.1 R/D conversion principle

This product adopted digital tracking method as R/D conversion system, and this method is one of the negative feedback control of closed-loop configuration, then it convert from Resolver analog signal to digital signal. A control deviation(ε) is shown in below equation, and it must be normally "0" with the negative feedback control system.

Control deviation : $\varepsilon = K \cdot \sin(\theta - \phi) \cdot \sin\omega t$

Here assuming "$\varepsilon = 0$" means "$\theta = \phi$", then Resolver analog angular signal can be converted to digital angular data.

■Configuration of digital tracking method R/D converter.



【Control deviation】: $\varepsilon = K \cdot \sin\theta \cdot \sin\omega t \times \cos\phi - K \cdot \cos\theta \cdot \sin\omega t \times \sin\phi$

$= K \cdot \sin(\theta - \phi) \cdot \sin\omega t$

$\varepsilon = 0 \quad \Rightarrow \quad \therefore \theta = \phi$

【Explanation of concept】

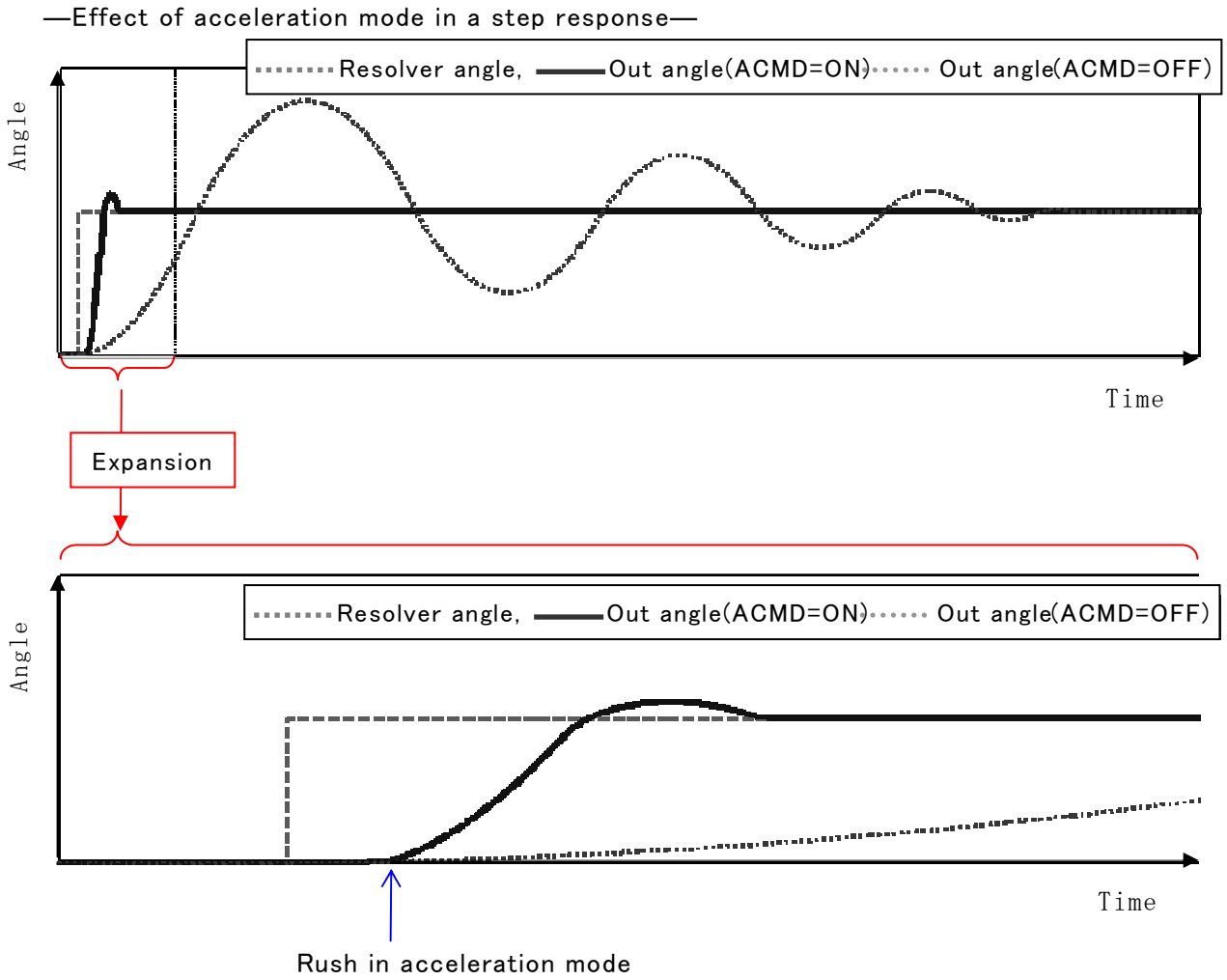
An amplitude modulated resolver signals enter to R/D converter. To calculate control deviation (ε), $\sin\theta$ modulated signal is multiplied by feedback $\cos\phi$ and $\cos\theta$ modulated signal is multiplied by feedback $\sin\phi$. This "ε" is encoded by comparator (Analog to Digital conversion), and $\sin\omega t$ component is removed by synchronous detection. Through a compensator which stabilize negative feedback loop and improve its characteristic (In general, compensator is PI control which configure with type Ⅱ direct servo loop.) , digital angular output ϕ can be generated as counter value.

10.2 Acceleration mode

An acceleration mode is the function to improve the dynamic performance more than primary characteristic and to be possible making more correct sensing according to switching of internal control mode against unexpected high angular acceleration. In this product, it is possible to set ON/OFF by ACMD terminal.

10.2.1 Effect of acceleration mode

After rapid change of resolver angle (high angle acceleration) happen, output angle will converge at a resolver angle. In case of acceleration mode is ON, output will soon be able to follow the resolver angle compare the case of mode=OFF. Cause of switching the internal control mode, rate of change angle is getting faster than mode=OFF condition. After following the angle of target output, control mode return to normal from acceleration mode.

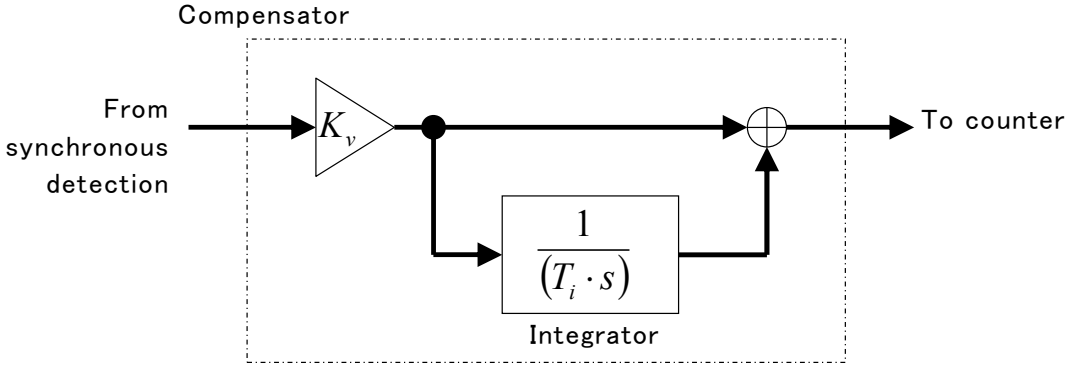


Refer specification P35 for detail about switching conditions entering to/releasing from acceleration mode.

10.2.2 Switching the internal control during acceleration mode

In this product, switching the internal control during acceleration mode is done by proportional gain switching of compensator.

■Compensator configuration



$$\text{(PI control element)} = K_v \cdot \left\{1 + \frac{1}{(T_i \cdot s)}\right\}$$

While, K_v : proportional gain, T_i : integration time constant, s : laplace operator

■Difference between normal mode and acceleration mode

Mode name	Explanation
Normal mode	Normal operation mode except the acceleration mode below.
Acceleration mode	High tracking rate mode by enlarging the proportional gain (K_v) by 32times of that in normal mode.

10.2.3 Considerations in the use of acceleration mode

(1)Change behavior when switching mode

It is considered that the acceleration mode does not occur frequently in usual operation except in special cases. But if it occurs actually by large angular acceleration is applied to the rotational axis, it may seem that some abnormal operation has occurred momentarily at observing the output waveform, cause the control loop gain suddenly change to 32 times.

(2)Miss-operation by noise and error

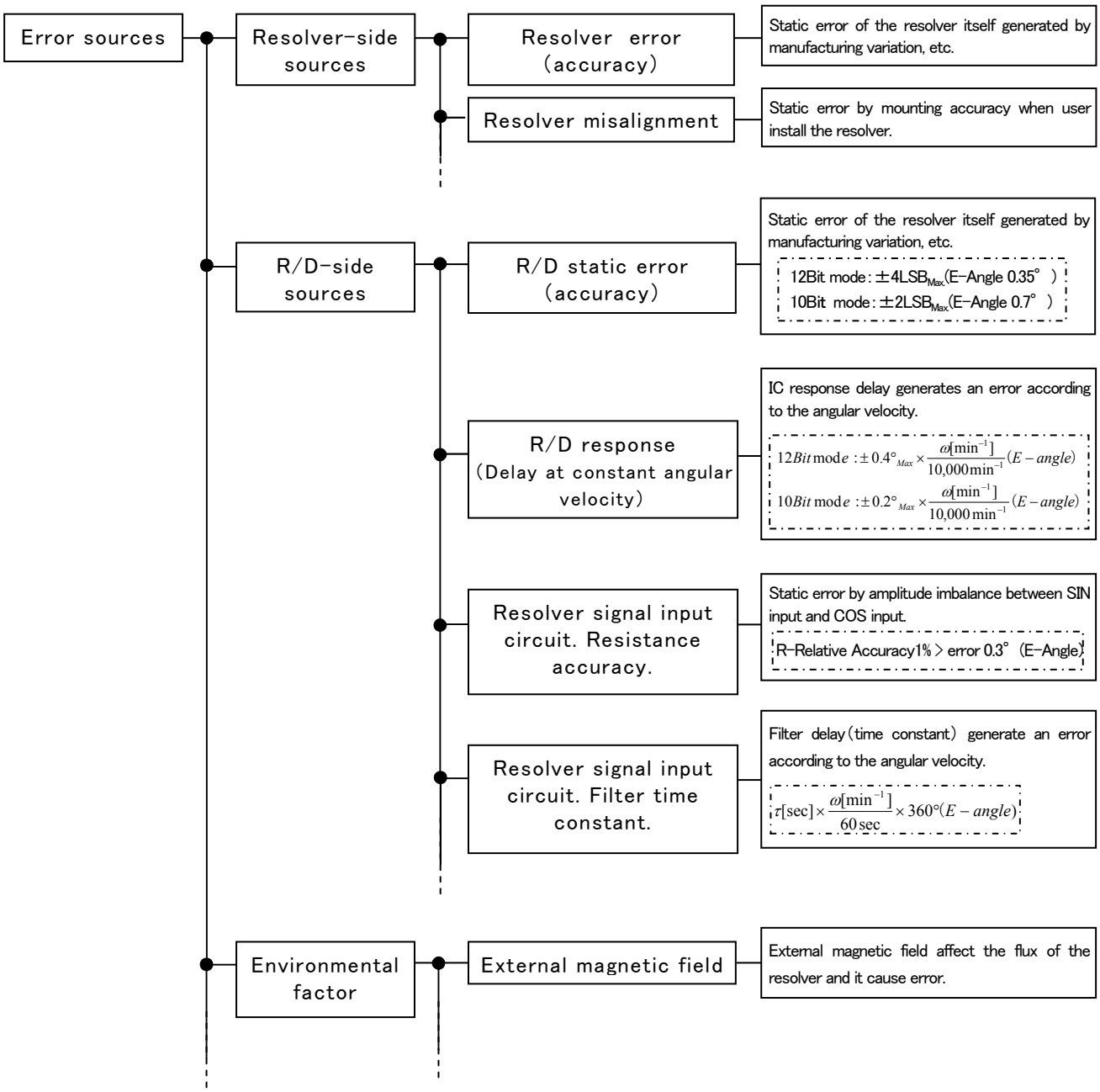
Note that even in the case that large angular acceleration does not apply, acceleration mode may occur due to excessive magnetic/electrical distortion of waveform, electrical error, noise in the resolver signals. If unexpected acceleration mode occurs by error or noise and your system have problem due to discontinuity of angular output data, please correspond by ACMD terminal setting. And refer specification for ACMD setting sequence.

10.3 About the error of resolver system

Resolver system with this product causes an error against actual angular position by resolver accuracy, this Smartcoder accuracy, peripheral configuration error, etc. In this chapter, explain the error sources of resolver system and general estimation method of total error.

10.3.1 Error sources

There are error sources of resolver system like the following.



10.3.2 Error estimates

Total error of the resolver system using this IC is a combination of potential errors which include static error that typically come from resolver itself or this IC itself, and proportional error of angular velocity that come from delay of this IC or peripheral circuit depending on the angular velocity.

$$\varepsilon_{TTL} = \varepsilon_{ST} + \varepsilon_{DLY} + \cdots$$

While ε_{TTL} : Total Error of resolver system
ε_{ST} : Static error of resolver system
ε_{DLY} : Angular velocity proportional error

※ Each error might have different unit, and there are concepts which are "Number of multiple", "Mechanical angle", "Electrical angle". (Refer section 10.5 for each term). When estimating the error, please be careful to fitting the unit.

■Estimation of static error

Considering the estimation method of resolver system static errors which include resolver accuracy and error of this IC itself and the variation of the peripheral circuit or configuration, the easiest way is taking the sum of the maximum error caused by factors. But it is difficult to assume a probability that all of errors will be worst value, considering process capability, etc. Also it might need excessive precision characteristic to satisfy system, then system cost might lead to increase.

Then static error of resolver system estimates normally with root mean square(RMS) method.

$$\varepsilon_{ST} = \sqrt{(\varepsilon_R)^2 + (\varepsilon_S)^2 + (\varepsilon_{RD})^2 + (\varepsilon_i)^2 \cdots}$$

While ε_{ST} : Static error of resolver system
ε_R : Error of resolver
ε_S : error of resolver misalignment
ε_{RD} : Static error of this IC itself
ε_i : Resolver signal input circuit :Resistance accuracy

■Estimation of angular velocity proportional error

Angular velocity proportional error of resolver system is caused by response delay of this IC and signal delay which depend on the filter circuit constructed in resolver input circuit. This error is getting bigger with higher angular velocity, and it is obtained by converting the angular displacement from total delay time at applied angular velocity. Then it is estimated as the sum of individual errors due to the delay factor.

$$\varepsilon_{DLY} = \varepsilon_{RDDLY} + \varepsilon_{FLTDLY} + \cdots$$

While ε_{DLY} : Angular velocity proportional error of resolver system
ε_{RDDLY} : Angle error of this IC response delay
ε_{FLTDLY} : Angle error of the filter time constant at resolver signal input circuit.

10.4 FAQ

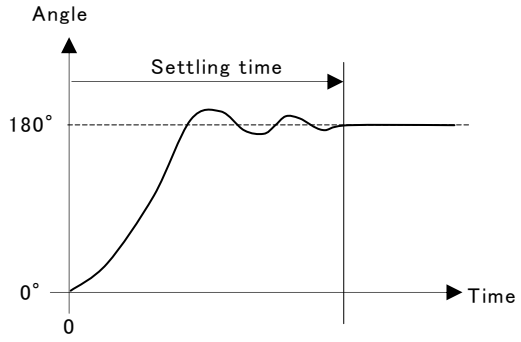
■Questions on the performance･characteristic of R/D conversion

Q.	How much time it takes to convert R/D？
A.	Assumed as delay time from input of resolver signal to output of its angle data. Then it will be as follows. ■Resolution 12Bit-mode：6.66μs max. ■Resolution 10Bit-mode：3.33μs max. Response spec is converted value from above time to the angular displacement of constant speed of rotation.

Q	What is the frequency (period) of the output data update rate?
A	It is 5MHz(200ns) while CLK input is 20MHz.

Q	Please tell us a frequency response of negative feedback loop which realize R/D conversion.
A	Bandwidth of control system is approximately as follows, and the response performance against a rapid angle change that is above following frequency is -40dB/dec characteristic. ■Resolution 12Bit-mode：800Hz. ■Resolution 10Bit-mode：1,200Hz

Q	What happen to the output data in case of resolver signal input is above maximum angular velocity?
A	R/D is unable to work tracking with angular velocity which is over specification, so it is unable to follow the rotation of the resolver. Then A,B,Z, and angle output Φ becomes irrelevant data.

Q	What is settling time？
A	The time to respond when resolver signal input change as step-like 180° . This is one of the indicators which shows control system performance of R/D converter. In normal operation, there is no chance to work this step(180°) response for the actual resolver signals. 

Q	In the operation of the rotating resolver, output angle data against actual resolver angle is shifted with the direction of rotation. Are there any considerable factor?
A	Typical factors are following. **(1)Displacement of the device which put on the resolver.** There might become angular displacement depending on direction, caused by mechanical misalignment of device like backlash of gear, etc. The problem of this factor is only depending on the rotation direction, and it is not depend on revolution speed of resolver. **(2)Time constant of filter circuit.** If resolver signal input to AU6802N1 through filters, there might show angular displacement depending on rotation direction while high speed resolver operation, caused by time constant delay value of filter circuit. The problem of this factor normally tends to be large in proportion to the number of revolution. **(3)Response of AU6802N1(Delay time of response):** Delay time from resolver signal input to corresponding angular data output might cause of the deviation angle which depend on the direction at high speed resolver operation. The problem of this factor normally tends to be large in proportion to the number of revolution.

■Questions about the resolver interface.

Q	Please tell the voltage specification of S1~S4 input signals.
A	Input signal voltage range of each terminals must be 0~VCC. For the signal level adjustment of operational setting, instead of adjusting terminal S1~S4, please adjust SINMNT/COSMNT voltage level which is 2~3Vp-p with COM potential center.

Q	Please tell us voltage specification of R1E-R2E(differential input) signals.
A	Input signal voltage range of each terminals must be 0~VCC. Regarding the differential signals (R1E-R2E), it is operational while there is potential difference. But it is recommended to apply over 4Vp-p, because applying higher voltage will be getting better comparator sensitivity.

Q	There has been recommended to add 470pF capacitor between RSO and COM. What happens if it does not exist?
A	A purpose of this capacitor is stability of the conversion. Without this capacitor, R/D output data will sometimes vibrate.

Q	As a noise countermeasure, would like to add normal-mode-capacitor C_N . How much capacitor value do you recommend?
A	C_N insertion is required as counter action for some negative effect of electrical noise injection. Actual cap value can not specify due to it depend on the noise level. Too large cap value might cause larger attenuation and phase change of resolver signals. So C_N value variability might cause an imbalance between SIN and COS, and it becomes error factor. Be careful about it.

Q	When adjusting the phase by input circuit of resolver exciting signals, are there any impacts on the response characteristic?
A	A response specification is a converted value of delaying time at electrical angle output. Then not affected.

Q	Specification said that phase difference between external exciting input(R1E-R2E) and resolver monitor signals(COSMNT, SINMNT) should be within ±10° . If phase difference is over ±10° , what kind of actual impact can we face?
A	When phase difference is over 10° , it takes time to settle angular output at startup, or in worst case it can not settle forever. Also when there is a steep angle change of resolver, IC might not be able to respond or takes long time to catch up. AU6802N1 are performing synchronous detection with reference the signal phase of external exciting input(R1E-R2E). Then such phase difference cause phase shift of synchronous detection. Equivalently negative feedback control loop gain that realize R/D conversion is getting decrease and dynamic transfer characteristic have some impact, so such symptoms appears.

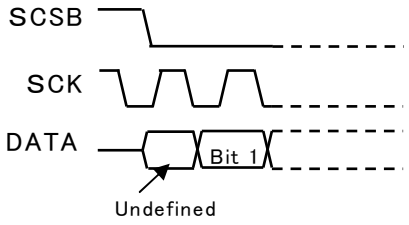
■Questions about the output interface.

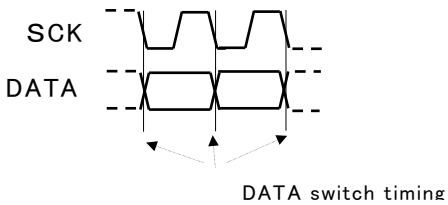
Q	In the situation of digital output terminals might be shorted each other , short to VDD or GND, what kind of issues will be appear when the power is active?
A	When the voltage is different between the shorted pin (One side “H” and other side “L”), excessive current flow from “H” to “L”, heating up, and finally IC might be damaged.

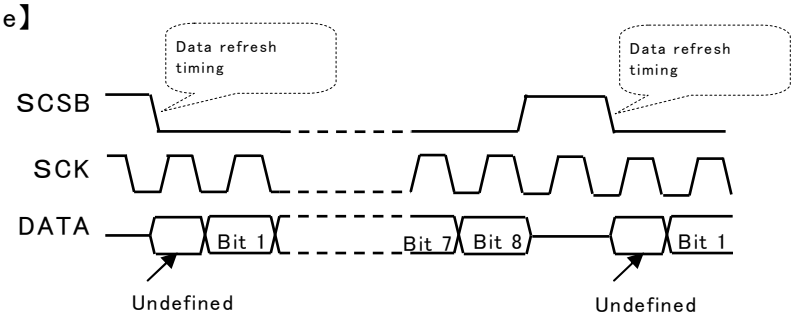
Q	Would like to get 8bit parallel output data. How can I do?
A	AU6802N1 have only 12bit-mode or 10bit-mode. When 12bit-mode, ignore the lower 4 bits. And when 10bit-mode, ignore the lower 2 bits then data will be looks like 8bit.

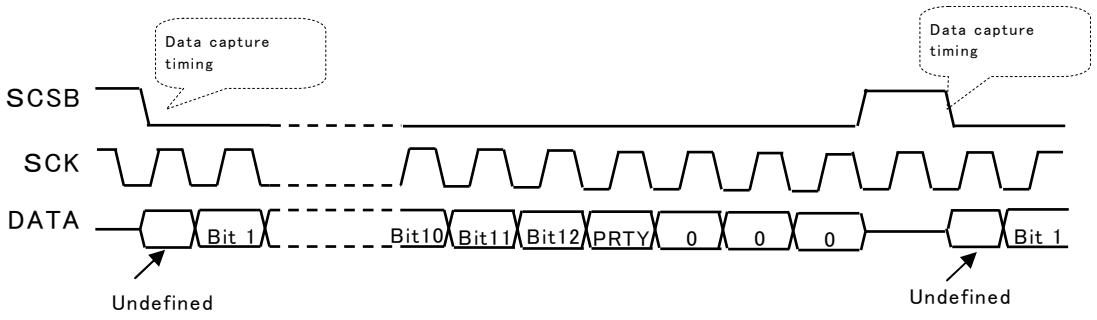
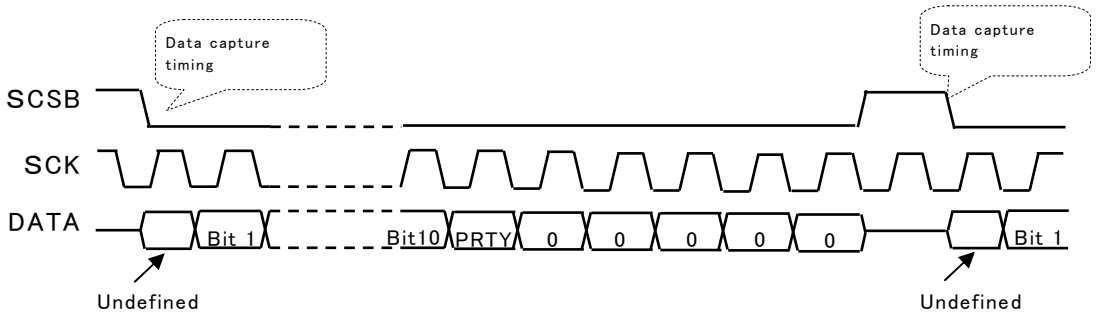
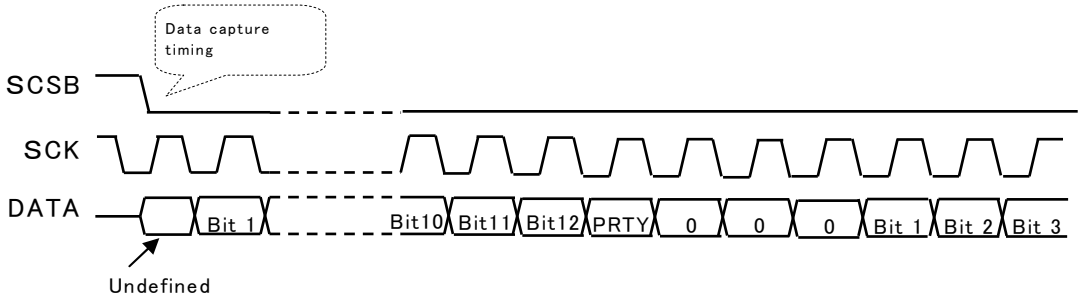
Q	Using encoder equivalent pulse mode, A/B pulse duty looks unstable while resolver rotate with same speed. What is possible cause?
A	Encoder equivalent pulse output of this IC is theoretically poorer performance than optical encoder pulse output. Due to the affect of resolver potential error and R/D potential error and also R/D conversion principle itself, it is possible to be disordered pulse duty even if in normal operation condition.

Q	For the digital output, serial interface output and parallel interface output are prepared. Both interfaces should be used?
A	Either one interface is enough and there are no problem for operation of this IC. According to the system environment, please use appropriate interface.

Q	In serial output case, after SCSB falling edge, is the data which is before first SCK falling edge unnecessary?
A	No need. After SCSB falling edge, output data which shows until SCK falling edge is undefined value. Please ignore it. 

Q	To read the serial output data with above system, which is better trigger? SCK rising edge or SCK falling edge?
A	Please use SCK rising edge. Serial output data change with SCK falling edge timing. Then if you read the data with SCK falling edge, there might read false data depending on read timing. 

Q	Plan to use serial output function. But data need only 8bit due to above system configuration. How should I handle about serial output data?
A	Please exit serial output sequence （SCSB=L⇒H） after 8th serial data output. ※Even in the middle to end, data is refreshed and next output mode start with MSB data. 【Example】 

Q	Plan to use serial output function. But data need 16bit width due to upper system configuration. How should I handle about serial output data?
A	While keeping “SCSB=L” and keeping SCK input beyond PRTY bit, please stop serial output sequence after 16th serial data output. If you continue adding SCK after PRTY bit while keeping “SCSB=L”, additional bit until 16th SCK takes 0 data and repeat the same data for each 16 SCK clock. **【Example of accuracy 12Bit-mode】**  **【Example of accuracy 10Bit-mode】**  **【In case of keeping SCK input while SCSB=L(with accuracy 12Bit-mode)】** 

■Questions about the digital input configuration.

Q	Regarding UVW pole number selection bits(XSEL1,XSEL2), Are these bits used for the absolute angle output mode of parallel out?
A	Do not use for the absolute angle output mode. Even if setting change between X1,X2,X3,X4, each absolute angle output shows one rotation data which means electrical angle 0～360° .

Q	A specification said that RSO output frequency selection pin setting (FSEL1=L、FSEL2=L) means VEL_MODE (10KHz). What kind of setting is this?
A	In VEL_MODE, D0～D11 output switch to the register value of internal operation. This setting is for internal method only. We recommend not to use it by customer.

Q	Would like to use accuracy 10bit mode. Is there no problem to startup with MDSEL=H ?
A	It is no problem while +5V(Power supply for IC:VCC、VDD) and the power supply for exciting amplifier of Resolver(V_{EXT}) are turned on at the same time. Or +5V is turned on later. Another sequence which +5V power turn on before the power supply for exciting amplifier on is not recommended to start up with 10bit-mode. If you would like to use 10bit-mode with this sequence, firstly start with 12bit-mode setting, and after completing initial follow-up you can change to 10bit-mode by MDSEL setting. (For detail, please refer p18～22 of specification.)

Q	Are there any notes in case of fixed off (ACMD=L) at acceleration mode?
A	Some instantaneous tracking delay or overshooting can not be avoided at the input of excessive angular acceleration by a sudden change of angular velocity or an external turbulence to the mechanical shaft of resolver(i.e. shock), etc. In the power-up sequence, when exciting amplifier power is faster or same time for AU6802N1 power-up, initial follow-up time will be extended from 20ms(max) which is ACMD=H case to 100ms(max). Also if exciting amplifier power is later than Au6802N1 power-up, initial follow-up time might need long time or inability to follow forever. For detail of acceleration mode, please refer section 10.2 .

Q	Are there any notes in case of fixed on (ACMD=H) at acceleration mode?
A	If acceleration mode occurs, it may seem that some abnormal operation has occurred momentarily at observing the output waveform, because the loop gain of control system changes significantly. Judgment of entering to acceleration mode depends on comparison between the deviation of control residual polarity and threshold value. Then even if non-actual operation which does not occur rotational acceleration at mechanical axis resolver, the acceleration mode may occur because following situations are acceleration condition from the perspective of R/D, like excessive magnetic distortion of waveform, or an electrical error in the Resolver signal, or some noise, etc. For detail of acceleration mode, please refer section 10.2 .

■Questions about the function of fault detection.

Q	Does the fault detection result affect the behavior of R/D conversion?
A	Does not affect. The fault detection function is independent to R/D conversion so fault detection result does not give a constraint on the output of R/D conversion. It will continue to operate R/D conversion as abnormal condition.

Q	When the error reset at ERRSTB, How long time do we need to set reset situation (ERRSTB=L) ?
A	Minimum 40ns (Same as maximum time to be extended ERRHLD signal).

Q	Does the error reset function by ERRSTB affect the behavior of R/D conversion?
A	Does not affect. ERRSTB is a function to reset ERRHLD output only.

Q	DC bias resistance was connected in reverse polarity. Nevertheless error detection looks work at signal disconnection situation. Why is the error detected?
A	Depending on the angle, there might be detected as error of abnormal sensor signal. Because they are connected in reverse polarity, in disconnection case, monitor output voltage expect shift to VCC-side. Then correct R/D conversion can not operate and it is considered that abnormality have been detected by error detection function of abnormal R/D conversion.

Q	When monitor output exceeds 3.5Vp-p, it is detected as fault. And are there any other negative effect?
A	It is considered about voltage saturation and abnormal waveform. They are getting to be the error factor of R/D conversion.

■Questions about the application.

Q	Is it possible to use with phase modulation type(BRT) resolver?
A	No. This product only support amplitude modulation type(BRX) resolver.

Q	Is it possible to use multiple AU6802N1 which connect same one resolver?
A	It is basically usable if same exciting signal input to each IC's R1E/R2E terminals. However in case of error at external exciting amplifier and RSO output abnormality of exciting signal source IC, all R/D system becomes unavailable. Note that it must be required to put capacitor between RSO and COM regardless RSO output use or not.

Q	How much cable length between resolver and AU6802N1 can we extend?
A	It can not to say simple because it depend on the type of cable and wiring, but basically there are not much problem about cable length itself which is a few meters except for noise superimposed, etc. Example for extremely long cable length is about 150m extended application exist and proven. Anyway it may require for phase adjustment or signal level adjustment, etc, because long cable might cause phase shift or amplitude change due to cable capacity.

10.5 Terms and Definitions

Term	Number of multiple(N)
Definition	Show 1/2 the number of poles(pole pair). Display is added with "X".

Term	Mechanical angle(θ m)
Definition	Rotational angle of resolver rotor(Machine axis)

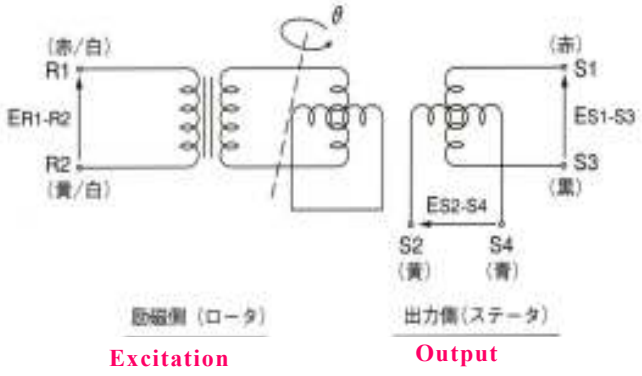
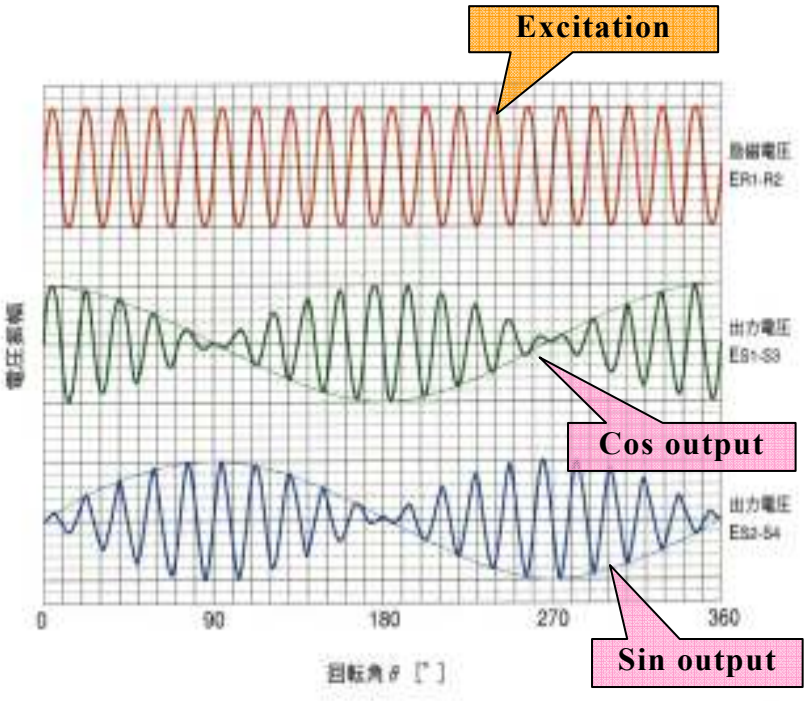
Term	Electrical angle(θ e)
Definition	Machine 1 cycle 360° /N(number of multiple) define as electrical 1 cycle 360°. $\Theta e = N \theta m$

Term	Exciting signal
Definition	Signal to be applied to the excitation winding of the resolver

Term	Resolver input impedance(Zro)
Definition	Resolver exciting-side impedance

Term	Resolver signal
Definition	Signal outputted from the output winding of resolver, when we applied the excitation signal.

Term	Resolver transformation ratio
Definition	Ratio of the excitation voltage and resolver signal maximum voltage

Term	BRX
Definition	1Phases/2Phases(Amplitude modulation type)brushless resolver. ■Configuration of resolver  ■Output equation Excitation : $E_{R1-R2} = E_1 \sin \omega t$ Output : $E_{S1-S3} = kE_1 \cos \theta \sin \omega t$ $E_{S2-S4} = kE_1 \sin \theta \sin \omega t$ ■Exciting signal and resolver signal waveform 

11. Revision history

Revised date	Revision	Revision content･reason
2013.05.10	First edition	−

スマートコーダ

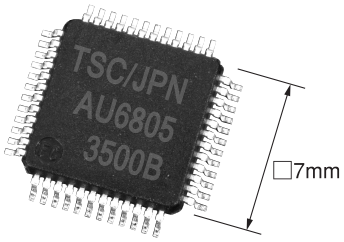
Smartcoder®

AU6805

レゾルバ／デジタル変換IC RESOLVER - TO -DIGITAL CONVERTER IC

デジタルトラッキング方式（リアルタイム絶対値角度変換）、
低価格・小型 高速12ビットR／D（レゾルバ／デジタル）変換IC

Digital-Tracking System (Real Time Absolute Angle Conversion)
Low cost/Small size High-speed 12Bit Resolver-to-Digital Converter IC



Smartcoder（スマートコーダ）はレゾルバ信号をデジタル絶対位置角度信号に変換するレゾルバ／デジタル変換ICです。弊社 Smartsyn（スマートシン）、Singlsyn（シングルシン）などのレゾルバと組み合わせて、自動車を始めロボット・工作機械に至るまで、幅広い分野での角度検出にご使用いただくことができます。

Smartcoder is an R/D (Resolver to Digital) conversion IC, which converts resolver signals into digital absolute position angle signals. It is usable in a wide range of applications, including vehicle/robot/machine-tool related applications, in combination with brushless resolvers such as our Smartsyn and Singlsyn.

■ 特長

■実績のあるデジタル・トラッキング方式のR/D変換を採用
■低価格・小型・軽量
■フェイルチェック機能の充実
　①異常検出機能
　　レゾルバ信号異常、レゾルバ信号断線、R/D変換異常、IC異常高温の検出が可能
　②自己診断機能（Built-In Self Test）搭載
　　R/D変換、異常検出動作を自らチェック
■オールインワン志向に基づく、システム・コストの低減を実現
　①励磁アンプ内蔵（出力電流：10mArms.／20mArms.）
　②動作クロック内蔵
■各種アプリケーションに対応した機能の充実
　①励磁信号の位相調整不要（許容範囲：±45° 以内）
　②制御帯域幅（f_{BW}）設定可変（固定値7種類と自動調整より選択）
　③リニアホールIC信号のデジタル変換や、レゾルバに対するR/Dの並列接続が可能
　④冗長角度出力（パラレル／パルス／シリアルの三重冗長）

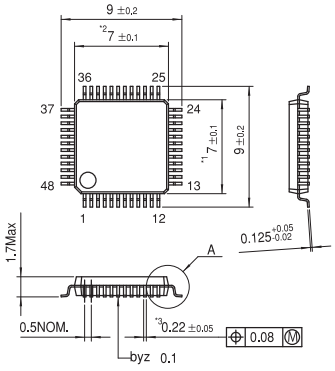
■ Features

■Adopts R/D conversion based on a proven digital-tracking system
■Low cost, small size and light weight
■Satisfying fail check functions
　①Abnormality detection
　　Capable of detecting abnormal resolver signals, breaking of resolver signals, abnormal R/D conversion and abnormally high temperature of an IC
　②Built-in self test
　　Conducts a self-test on R/D conversion and abnormality detection
■Realization of system/cost reduction based on all-in-one concepts
　①Integrated with an excitation amplifier (Output current : 10mA rms/20mA rms)
　②Integrated with an operation clock
■Enhancement of functions corresponding to various applications
　①Requires no phase adjustment to excitation signals (Allowable range: Within±45°)
　②Variable setting of controlling bandwidth (f_{BW})
　　(Selectable from 7 types of fixed values or automatic adjustment)
　③Capable of digital conversion of linear hall IC signals and R/D parallel connections to resolvers
　④Output redundancy (Triple redundancy - Parallel/Pulse/Serial output)

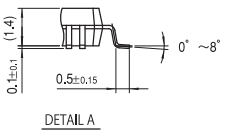
■ 仕様 Specifications

分　解　能 Resolution	4,096（$=2^{12}$）
追 従 速 度 Tracking rate	240,000rpm（f_{BW}固定時） 240,000rpm（When f_{BW} is fixed.）
変 換 精 度 Conversion accuracy	±4 LSB
最 大 加 速 度 Max. angular acceleration	3,000,000 rad/sec^2（f_{BW}自動調整時） 3,000,000 rad/sec^2（When f_{BW} is automatic adjustment.）
セトリングタイム Settling time	1.5ms（180° 入力ステップ、f_{BW}自動調整時） 1.5ms（When input step is 180°, and f_{BW} is automatic adjustment.）
出 力 応 答 性 Output response	±0.2°／10,000rpm
出　力　形　態 Output form	12ビット2進コード　正論理パラレル +A,B,Z +シリアルI/F 12bit binary code Positive logic parallel + A,B,Z + Serial I/F
所 要 電 源 Power requirement	+5V±10%（45mA：励磁アンプ10mArms.設定時） +5V±10%（45mA: When the excitation amplifier is set at 10mA rms.）
励 磁 電 源 Excitation power supply	定電流制御方式励磁アンプ内蔵（10mArms / 20mArms） Integrated with a constant current control method excitation amplifier（10mArms / 20mArms）
外 形 寸 法 Outline	48ピンLQFP（7×7）、ピン間隔：0.5mm 48 pin LQFP (7×7) Pin to pin: 0.5mm
動 作 温 度 Operating temperature	−40℃ ～ +125℃

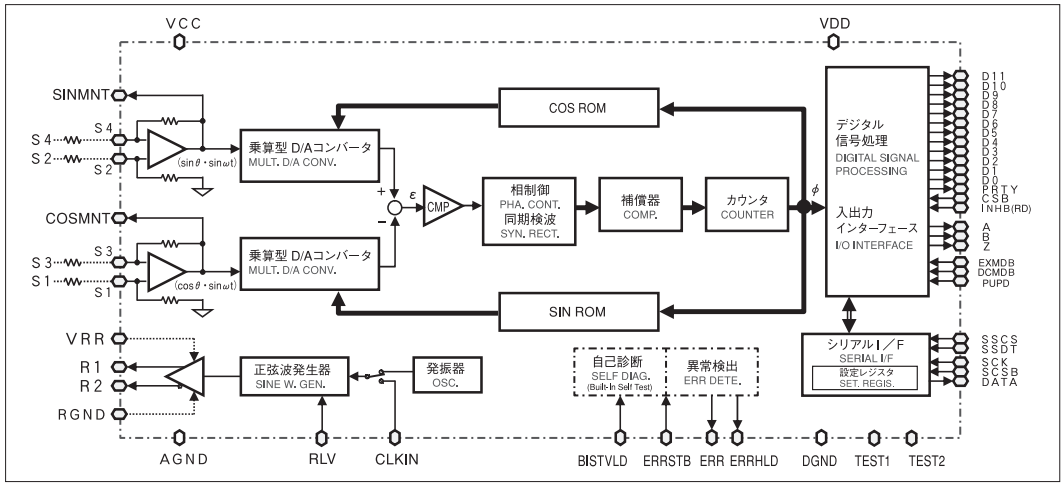
■ 外形図 Outline



*1、*2･･･レジン残りは含まない。
Remaining resin is not included.
*3･･･タイバー残りは含まない。
Remaining tie bar is not included.



■ 構成図
Functional Block Diagram



■ 入出力信号一覧 Pin description

NO.	信号名称 Symbol	種類 Class	備考 Remarks
1	EXMDB	D/I	外部励磁信号源モード：Ext. excit. sig. source mode
2	DCMDB	D/I	DCレゾルバモード：DC resolver mode
3	RLV	D/I	励磁電流選択：Excitation current select
4	VCC	——	アナログ電源：Analog power supply
5	SINMNT	A/O	SINモニター：SIN monitor
6	COSMNT	A/O	COSモニター：COS monitor
7	AGND	——	アナログGND：Analog GND
8	S3	A/I	S3入力：S3 input
9	S1	A/I	S1入力：S1 input
10	S2	A/I	S2入力：S2 input
11	S4	A/I	S4入力：S4 input
12	R GND	——	励磁アンプGND：Excitation amp. GND
13	R2	A/O(I)	励磁出力R2：Excitation output R2
14	VRR	——	励磁アンプ電源：Excitation amp. PS
15	R1	A/O(I)	励磁出力R1：Excitation output R1
16	BISTVLD	D/I	BIST実行制御：BIST execution control

NO.	信号名称 Symbol	種類 Class	備考 Remarks
17	CLKIN	D/I	クロック入力：Clock input
18	SSDT	D/I	シリアル設定データ：Serial setting data
19	SSCS	D/I	シリアル設定CS：Serial setting CS
20	DATA	D/O(BUS)	シリアルデータ：Serial data
21	SCSB	D/I	シリアルCSB：Serial CSB
22	PRTY	D/O(BUS)	パリティ：Parity
23	SCK	D/I	シリアルクロック：Serial clock
24	DGND	——	デジタルGND：Digital GND
25	D11	D/O(BUS)	ERRCD3／ϕ1
26	D10	D/O(BUS)	ERRCD2／ϕ2
27	D9	D/O(BUS)	ERRCD1／ϕ3
28	D8	D/O(BUS)	ERRHLD／ϕ4
29	D7	D/O(BUS)	ERR／ϕ5
30	D6	D/O(BUS)	—／ϕ6
31	D5	D/O(BUS)	W相／ϕ7 ：Phase W／ϕ7
32	D4	D/O(BUS)	V相／ϕ8 ：Phase V／ϕ8

NO.	信号名称 Symbol	種類 Class	備考 Remarks
33	D3	D/O(BUS)	U相／ϕ9 ：Phase U／ϕ9
34	D2	D/O(BUS)	Z相／ϕ10 ：Phase Z／ϕ10
35	D1	D/O(BUS)	B相／ϕ11 ：Phase B／ϕ11
36	D0	D/O(BUS)	A相／ϕ12 ：Phase A／ϕ12
37	VDD	——	デジタル電源：Digital PS
38	INHB(RD)	D/I	インヒビット：Inhibit
39	ERRHLD	D/O(I)	エラー（保持）：Error (Hold)
40	ERRSTB	D/I	エラーリセット：Error reset
41	ERR	D/O(I)	エラー出力：Error output
42	A	D/O	A相パルス出力：Phase A pulse output
43	B	D/O	B相パルス出力：Phase B pulse output
44	Z	D/O(I)	Z
45	CSB	D/I	チップセレクト：Chip select
46	PUPD	D/I	パラレル絶対値更新切換：Paral. abs. upd. sw.
47	TEST1	D/I	（テストモード設定）：Test mode setting
48	TEST2	D/I	（テストモード設定）：Test mode setting

（注） 1. “No.” は、端子（ピン）No.に対応する。“No.” is corresponding to the pin number of terminal.
2. 信号種類は、以下による。“Class” means as follows:
＊A/Iアナログ入力 A/I: Analog input ＊A/Oアナログ出力 A/O: Analog output ＊A/O(I)アナログ出力(制御端子入力にて入出力切換) A/O (I): Analog output (I/O is switched by control terminal input.)
＊D/Iデジタル入力 D/I: Digital input ＊D/Oデジタル出力 D/O: Digital output ＊D/O(I)デジタル出力(内部にて入力付加) D/O (I): Digital output (Input is added internally.) ＊D/O(BUS)デジタル出力(3-state出力) D/O (BUS): Digital output (3-state output)
3. No.47のTEST1信号及びNo.48のTEST2信号は、運用には直接関与しない信号であり、通常は、TEST1はデジタル電源（VDD）と、TEST2はデジタルGND(DGND)と短絡しておく。
何も接続しない場合は内部でそれぞれプルアップまたはプルダウンされる。TEST1 signal in No.47 and TEST2 signal in No.48 do not affect the operation directly, and TEST1 should usually be connected to the digital PS (VDD), and TEST2 to the digital GND (DGND). When they are not connected to, they are internally pulled up or pulled down respectively.

Tamagawa® 多摩川精機株式会社

販売会社

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⚠ 安全に関するご注意

●正しく安全にお使いいただくため、ご使用の前に「安全上のご注意」をよくお読みください。

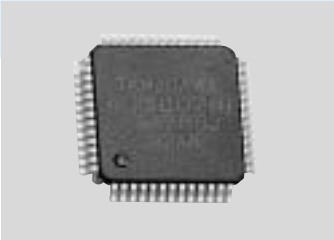
製品の保証

製品の無償保証期間は出荷後一年とします。ただし、お客様の故意または過失による品質の低下を除きます。なお、品質保持のための対応は保証期間経過後であっても、弊社は誠意をもっていたします。弊社製品は、製品毎に予測計算された平均故障間隔(MTBF)は極めて長いものでありますが、予測される故障率は零(0)ではありませんので弊社製品の作動不良等で考えられる連鎖または波及の状況を考慮されて、事故回避のため多重の安全策を御社のシステムまたは／および製品に組み込まれることを要望いたします。

■本カタログのお問い合わせは下記へお願いします。
・商品のご注文は、担当営業本部またはお近くの営業所までお問い合わせください。
・技術的なお問い合わせは、
モータトロニクス研究所
センサ技術課　直通　TEL(0265)56-5433
FAX(0265)56-5434

本カタログに記載された内容は予告なしに変更することがありますので御了承ください。
T12-1704　1,000部　初版印刷　2014年12月10日.
'14.12
本カタログの記載内容は2014年12月現在のものです。

●インターネットホームページ
http://www.tamagawa-seiki.co.jp



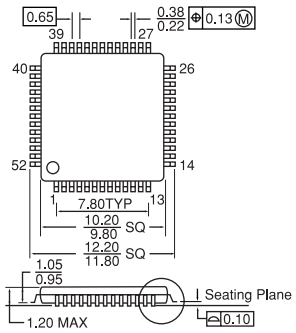
Model : AU6802N1

Features

(1) Applicable to all of our resolvers. (1 phase excitation 2 phase output)
(2) Vehicle-mount quality
- ●Quality level : Transportation equipment involved in safety
- ●Operating temperature range : −40～+125℃

(3) High accuracy
(4) Simple to use
- ●Real time output (High tracking rate : 240,000min^{-1}/10bit resolution)
- ●Single power supply of DC5V (Integrated oscillator for exciting resolver : 10/20KHz)
- ●Small size and light weight (10×10mm, pin interval : 0.65mm, 52pin TQFP, Mass 0.3g)
- ●Built-in test (Internal error detection) function
- ●Pulse / Parallel / Bus + Serial output (Selectable)
- ●Capable of setting a number of poles for UVW (Selectable from×1,2,3,4)
- ●Clock input (20MHz) : External CLK input / Crystal resonator / Ceramic resonator (Selectable)
- ●Resolution of 10/12 bit (Selectable)

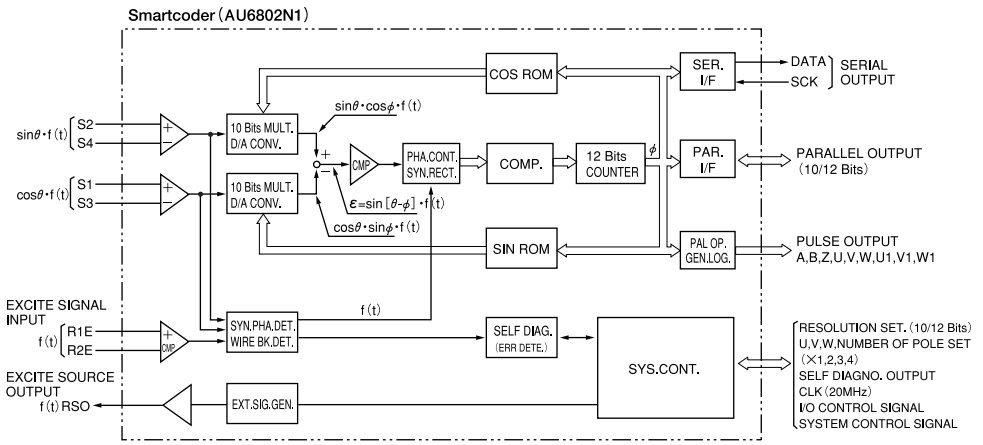
Outline



Specifications

Output form	Binary code parallel 10/12 bit bus compatible, positive logic	
Resolution	1,024 (2^{10})	4,096 (2^{12})
Tracking rate	240,000min^{-1}	60,000min^{-1}
Conversion accuracy	±2LSB	±4LSB (21′)
Settling time (For step input of 180° in electric angle)	1ms Typ. (ACMD="H")	2.5ms Typ. (ACMD="H")
Response (As output response delay in electric angle)	±0.2° Max./10,000min^{-1}	±0.4° Max./10,000min^{-1}
2 phase pulse signal (A,B)	256C/T	1,024C/T
Source dissipation	DC5V±5% 45mA Max. (30mA Typ.)	
Operating temperature	−40～+125℃	
Storage temperature	−65～+150℃	
Humidity	90%Rh Max.	
Mass	1g Max.	

Functional Block Diagram



Pin Description

Pin No.	Symbol	Form	Function
1	R1E	A/I	EXT.EXCIT.IP.
2	R2E	A/I	(DIF.IP.)
3	VCC	—	ANALOGUE SOURCE
4	SINMNT	A/O	SIN.MONITOR
5	S4	A/I	SIN.IP.
6	S2	A/I	(DIF.IP.)
7	A GND	—	ANALOGUE GND
8	S1	A/I	COS.IP.
9	S3	A/I	(DIF.IP.)
10	COSMNT	A/O	COS.MONITOR
11	VCC	—	ANALOGUE SOURCE
12	RSO	A/O	SIG.FOR EXCIT.
13	COM	A/O	COMMON (2.5V)

Pin No.	Symbol	Form	Function
14	A GND	—	ANALOGUE GND
15	MDSEL	D/I	RES.SELECT
16	ACMD	D/I	ACCEL.MODE CONTROL
17	XSEL1	D/I	UVW P SEL.
18	XSEL2	D/I	
19	OUTMD	D/I	OP.SEL
20	SCSB	D/I	SERIAL CSB.
21	DATA	D/O	SERIAL DATA
22	SCK	D/I	SERIAL LOCK
23	VDD	—	DIGITAL SOURCE
24	XTAL	—	OSC.CONN.
25	CLKIN	D/I	EXTERNAL CLK INPUT
26	D GND	—	DIGITAL GND

Pin No.	Symbol	Form	Function
27	D0	D/O (BUS)	PRTY/φ12
28	D1	D/O (BUS)	ERRHLD/φ11
29	D2	D/O (BUS)	ERR/φ10
30	D3	D/O (BUS)	W1/φ9
31	D4	D/O (BUS)	V1/φ8
32	D5	D/O (BUS)	U1/φ7
33	D GND	—	DIGITAL GND
34	D6	D/O (BUS)	Wch./φ6
35	D7	D/O (BUS)	Vch./φ5
36	D8	D/O (BUS)	Uch./φ4
37	D9	D/O (BUS)	Zch./φ3
38	D10	D/O (BUS)	Bch./φ2
39	D11	D/O (BUS)	Ach./φ1

Pin No.	Symbol	Form	Function
40	D GND	—	DIGITAL GND
41	CSB	D/I	CHIP SELECT
42	RDB	D/I	LEAD
43	INHB (RD)	D/I	INHIBIT
44	PRTY	D/O (BUS)	PARITY
45	ERRHLD	D/O	ERROR HOLD
46	ERRSTB	D/I	ERROR RESET
47	FSEL1	D/I	FREQUENCY SELECT
48	FSEL2	D/I	FREQUENCY SELECT
49	VDD	—	DIGITAL SOURCE
50	TEST1	D/I	TEST MODE SET
51	TEST2	D/I	TEST MODE SET
52	A GND	—	ANALOGUE GND

Note : *A/I ANALOG INPUT. *A/O ANALOG OUTPUT. *D/I DIGITAL INPUT. *D/O DIGITAL OUTPUT.